

| PAGE | TITLE | Quantity |
|------|-------------------------------|----------|
| 01 | COVER PAGE | |
| 02 | BLOCK DIAGRAM | |
| 03 | CPU (PCIE/DMI) | |
| 04 | CPU (DDI/EDP) | |
| 05 | CPU (DDR) | |
| 06 | CPU (SVID/CFG/JTAG/CLK) | |
| 07 | CPU (VCORE/VCCGT) | |
| 08 | CPU (CCSA/VCCIO/VDDQ/RSVD) | |
| 09 | CPU (VSS) | |
| 10 | CPU (Power CAP) | |
| 11 | CPU (Power Cap2) | |
| 12 | DDR (DDR4-CHA) | |
| 13 | DDR (DDR4-CHB) | |
| 14 | DDR (RSVD) (DDR4-CHA1) | |
| 15 | PCH (SPI/UART/I2C) | |
| 16 | PCH (DMI/PCI-E/USB)DDI GP | |
| 17 | PCH (PCI-E/SATA) | |
| 18 | PCH (CLOCK/CL) | |
| 19 | PCH (USB/ESPI) | |
| 20 | PCH(GPIO/CPU/SMBUS/IHDA/JTAG) | |
| 21 | PCH (POWER1) | |
| 22 | PCH (POWER2) PCH Strap | |
| 23 | PCH Power CAP | |
| 24 | ECIO (ITE8732F CX) | |
| 25 | Flash&RTC | |
| 26 | INT IO (Thermal/FAN) | |
| 27 | AUDIO (RSVD) (ALC286) | |
| 28 | Audio (RSVD) (AMP) | |
| 29 | Audio (RSVD HP/SPK/MICJack) | |
| 30 | Audio (RSVD) | |
| 31 | LAN (RTL8111GA) | |
| 32 | RJ45&Transformer (R) | |
| 33 | Card reader (R) | |
| 34 | USB3 Redriver(PI3EQX1012C) | |
| 35 | USB (RSVD) | |
| 36 | USB (USB Power Switch) | |
| 37 | USB (HEADER CAM/TOUCH) | |
| 38 | USB (USB30 PORT) | |
| 39 | Sequence (RSVD) | |
| 40 | Sequence (Power Plane EN) | |
| 41 | Sequence (Power5V&3.3V) | |
| 42 | INT IO (RSVD) | |
| 43 | INT IO (DCIN JACK) | |
| 44 | Power (OZ554 LED Converter) | |
| 45 | Power (5V/3D3V RT6575D) | |
| 46 | Power (NCP81203 CPUCORE1/1) | |
| 47 | Power (NCP1151 CPUCORE1/2) | |
| 48 | Power (NCP81151 CPUVGT1/3) | |
| 49 | Power (NCP1589A DCDC12V) | |
| 50 | Power (RT8231A VDDQ/VTT) | |
| 51 | Power (RT8237C PCH1P0V) | |
| 52 | Power (RT8237C VCC SA) | |
| 53 | Power (RT8237C VCC IO) | |
| 54 | Power (LDO 1P5V 2P5V) | |

| PAGE | TITLE | Quantity |
|------|-----------------------------|----------|
| 55 | LVDS Connector | |
| 56 | HDMI IN | |
| 57 | HDMI OUT | |
| 58 | DVI/CRT (R) | |
| 59 | Display switch (R) | |
| 60 | HDD/ODD | |
| 61 | Mini PCIE Card TV Tuner (R) | |
| 62 | WLAN and BT--NGFF | |
| 63 | SSD-NGFF | |
| 64 | PWR BT/Side Key/LED | |
| 65 | Stand off&EMI Cap&DUMMY BOM | |
| 66 | IO Board | |
| 67 | COM (R) | |
| 68 | Debug | |
| 69 | LPT (R) | |
| 70 | G sensor (R) | |
| 71 | Thunderbolt (R) | |
| 72 | Thunderbolt (R) | |
| 73 | Thunderbolt (R) | |
| 74 | Thunderbolt (R) | |
| 75 | Thunderbolt (R) | |
| 76 | GPU (1/5): PEG | |
| 77 | GPU (2/5): DIGITALOUT | |
| 78 | GPU (3/5): VRAM I/F | |
| 79 | GPU (4/5): GPIO/STRAP | |
| 80 | GPU (5/5): PWR/GND | |
| 81 | VRAM1 (1/2) | |
| 82 | VRAM2 (3/4) | |
| 83 | VRAM3 (5/6) | |
| 84 | VRAM4 (7/8) | |
| 85 | GPU CORE NVVDD(RT8812AGQW) | |
| 86 | DISCRETE VGA POWER | |
| 87 | GPU Switch (R) | |
| 88 | GPU Switch (R) | |
| 89 | GPU others (R) | |
| 90 | NFC (R) | |
| 91 | TPM (R) | |
| 92 | PS2 (R) | |
| 93 | Express Card (R) | |
| 94 | Smart Card (R) | |
| 95 | Scalar-RTD2506S | |
| 96 | Scalar Power | |
| 97 | Inter LAN (R) | |
| 98 | LAN Switch (R) | |
| 99 | XDP&ITP | |
| 100 | Table of Content | |
| 101 | GPIO table | |
| 102 | POWER SEQUENCE | |
| 103 | Power Block Diagram | |
| 104 | SMBUS table | |
| 105 | CLOCK MAP | |
| 106 | RESET Flow CHART | |
| 107 | Change History | |

Model: AIO, Petra238i
SCH Ver: 1A
PCB Ver:1A
PCB NumSAber:17567
PCB P/N:
3PD0BD010001

PCB BOARD SIZE
6 Layers
237mmX182mm

BOM Configuration
Unmount : (R_)

GPU: (G_)
(N17S_)
(N16S_)

NonGPU : (U_)

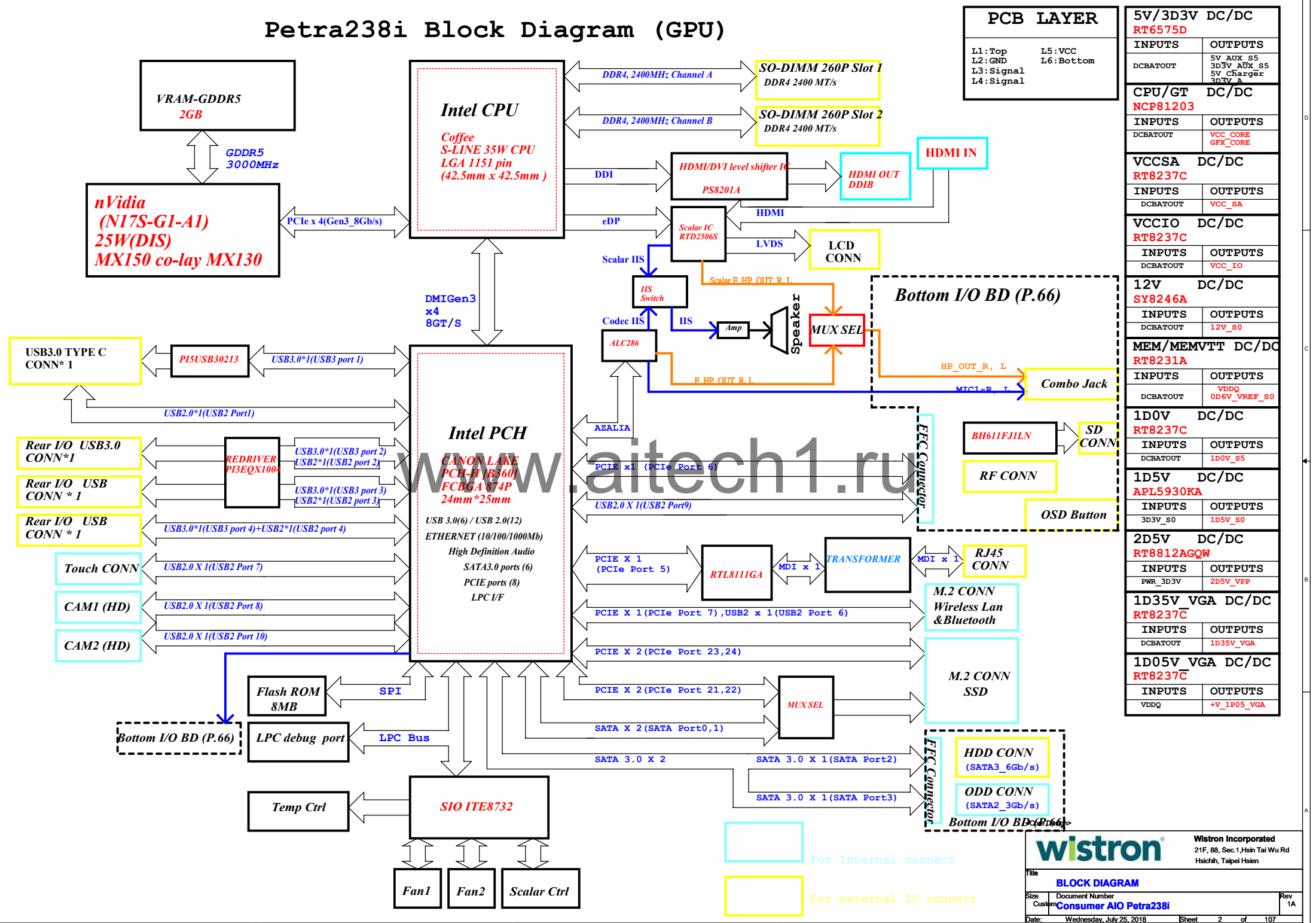
Hynix VRAM: (H_)
MICRON VRAM: (M_)

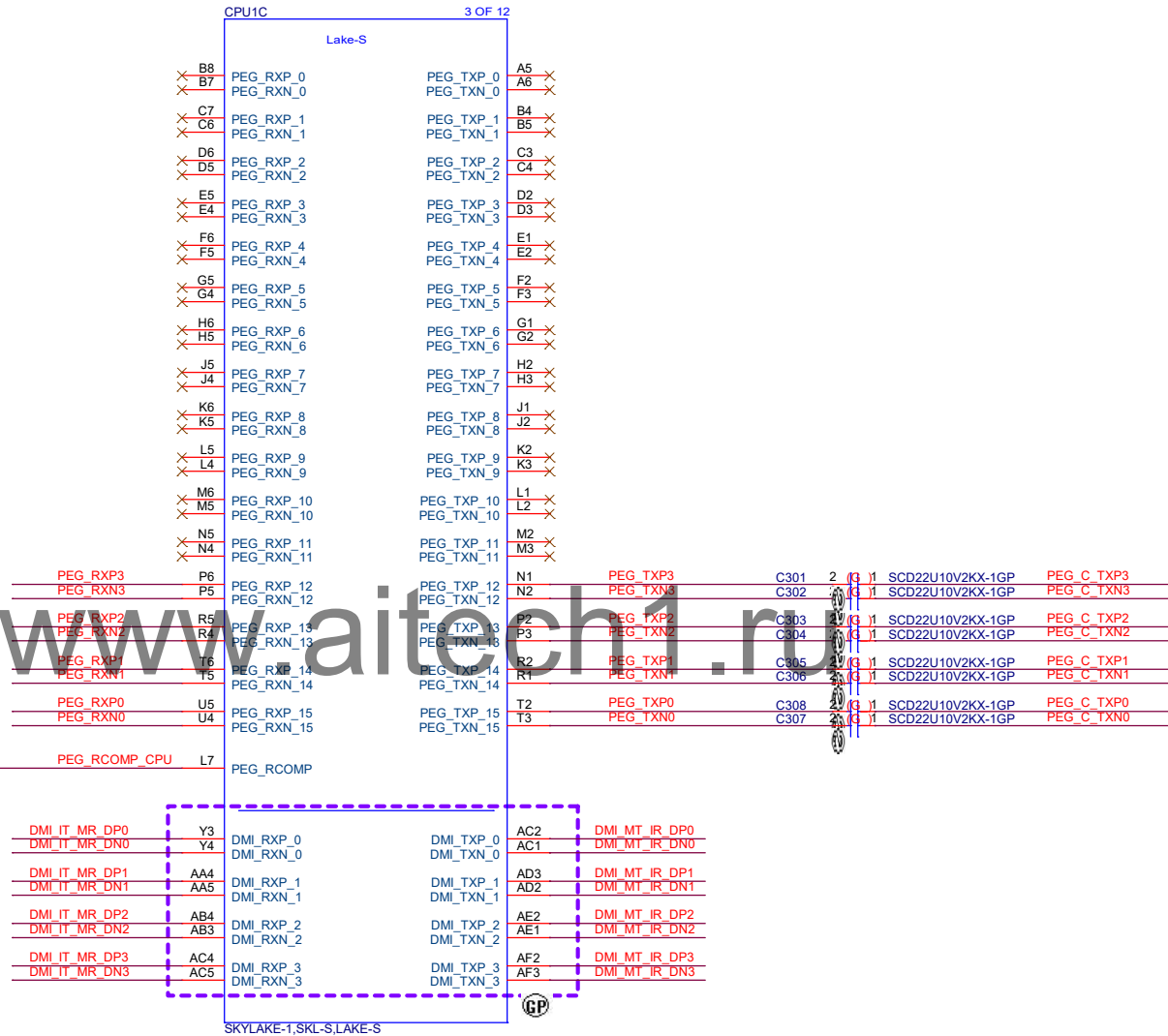
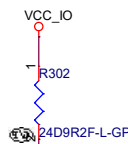
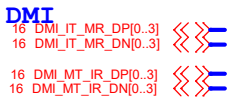
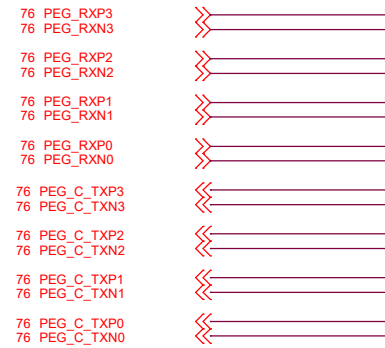
CPU 62 : (S62_)
NONS62: (NONS62_)

Modern Standby :
(MS_)
(NONMS_)

Modern Standby Test:
(MST_)

Petra238i Block Diagram (GPU)

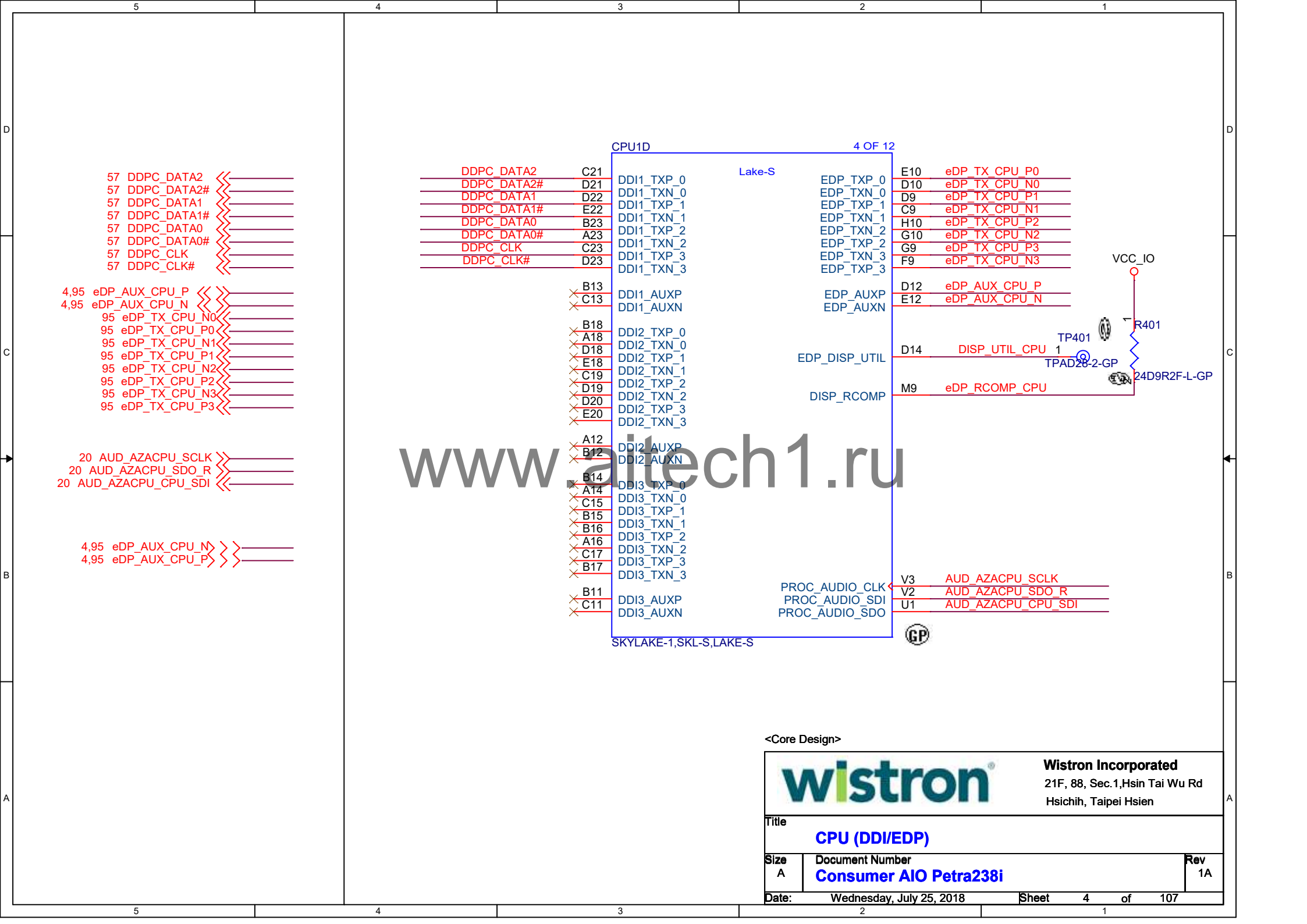




reverse at PCH side

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| | | Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Hsichih, Taipei Hsien | |
| Title CPU(PCIE/DMI) | | | |
| Size Custom | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: Wednesday, July 25, 2018 | Sheet 3 | of 107 | |



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Title

CPU (DDI/EDP)

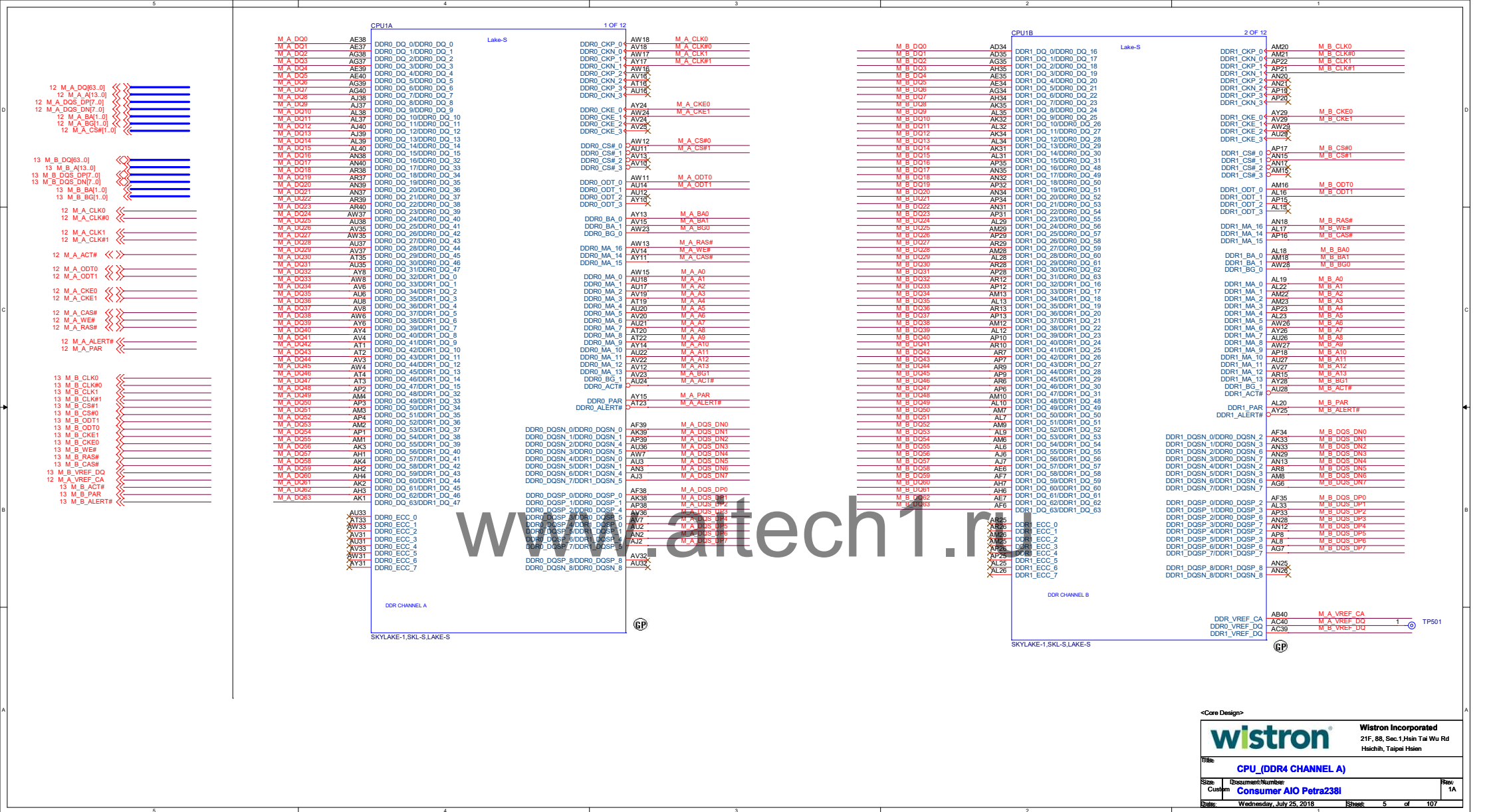
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Document Number
Consumer AIO Petra238i

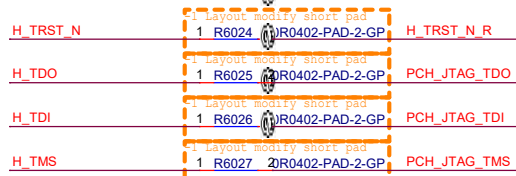
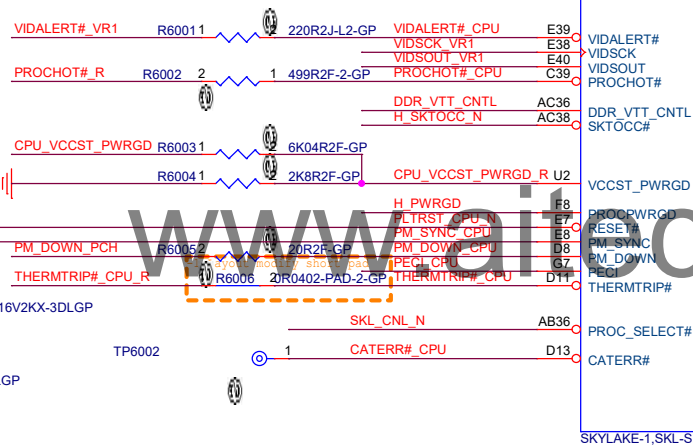
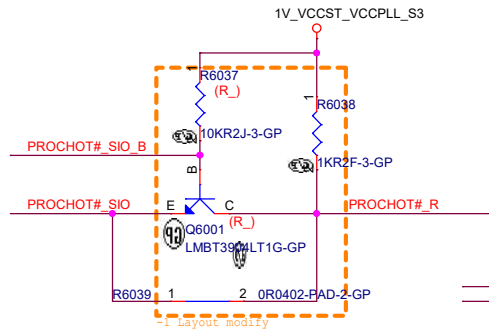
Rev
1A

Date: Wednesday, July 25, 2018

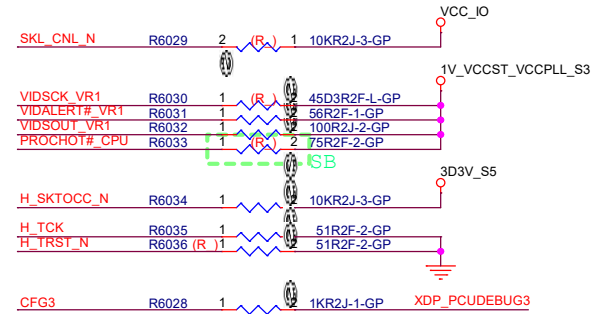
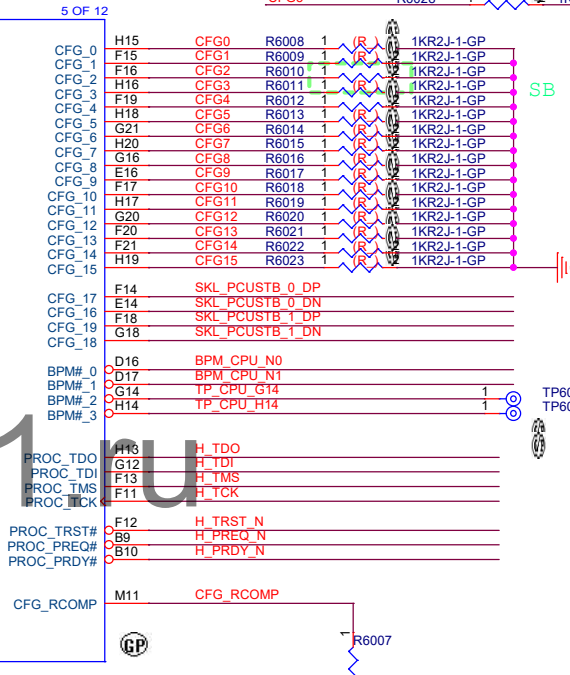
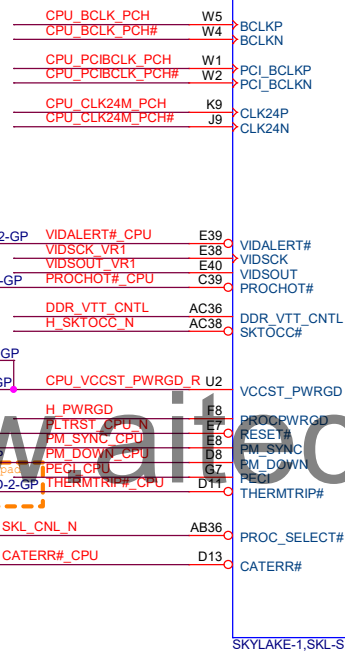
Sheet 4 of 107



6,99 XDP_PCUDEBUG3 >>>
99 CFG[0..15] >>>
99 SKL_PCUSTB_0_DP >>>
99 SKL_PCUSTB_0_DN >>>
99 SKL_PCUSTB_1_DP >>>
99 SKL_PCUSTB_1_DN >>>
99 BPM_CPU_N0 >>>
99 BPM_CPU_N1 >>>
99 H_TDO >>>
99 H_TDI >>>
99 H_TMS >>>
20,99 H_TCK >>>
65,99 H_TRST_N >>>
99 H_PREQ_N >>>
99 H_PRDY_N >>>
46 VIDSCK_VR1 >>>
46 VIDSOUT_VR1 >>>
46 VIDALERT#_VR1 >>>
18 CPU_BCLK_PCH >>>
18 CPU_BCLK_PCH# >>>
18 CPU_PCBCLK_PCH >>>
18 CPU_PCBCLK_PCH# >>>
18 CPU_CLK24M_PCH >>>
18 CPU_CLK24M_PCH# >>>
24,43 PROCHOT#_SIO <<<
65 CPU_VCCST_PWRGD_R <<<
46 PROCHOT#_R >>>
50 DDR_VTT_CNTL >>>
40,99 CPU_VCCST_PWRGD >>>
20,65,99 H_PWRGD >>>
17,65,99 PLTRST_CPU_N >>>
17 PM_SYNC_CPU >>>
17 PM_DOWN_PCH <<<
17,24 PECL_CPU <<<
17,79 THERMTRIP#_CPU_R <<<
17 H_SKT0CC_N <<<
20 PCH_JTAG_TDO >>>
20 PCH_JTAG_TDI >>>
20 PCH_JTAG_TMS >>>
21 H_TRST_N_R >>>
6,99 XDP_PCUDEBUG3 <<<



| Signal Name | Description | Dir. | Buffer Type | Link Type | Availability |
|-------------|---|------|-------------|-----------|--|
| CFG[19:0] | Configuration Signals: The CFG signals have a default value of 1 if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins: • CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted. = 1 = (Default) Normal Operation; No stall. = 0 = Stall. • CFG[1] : Reserved configuration lane. • CFG[2] : PCI Express* Static x16 Lane Numbering Reversal. = 1 = Normal operation = 0 = Lane numbers reversed. • CFG[3] : Reserved configuration lane. • CFG[4] : xDP enable: = 1 = Disabled. = 0 = Enabled. • CFG[6:3] : PCI Express* Bifurcation = 00 = 1 x8, 2 x4 PCI Express* = 01 = reserved = 10 = 2 x8 PCI Express* = 11 = 1 x16 PCI Express* • CFG[7] : PEG Training: = 1 = (default) PEG Train immediately following RESET# de assertion. = 0 = PEG Wait for BIOS for training. • CFG[19:8] : Reserved configuration lanes. | 1 | GTL | SE | All Processor Lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-Processor. Line only and test point may be placed on the board for them. |



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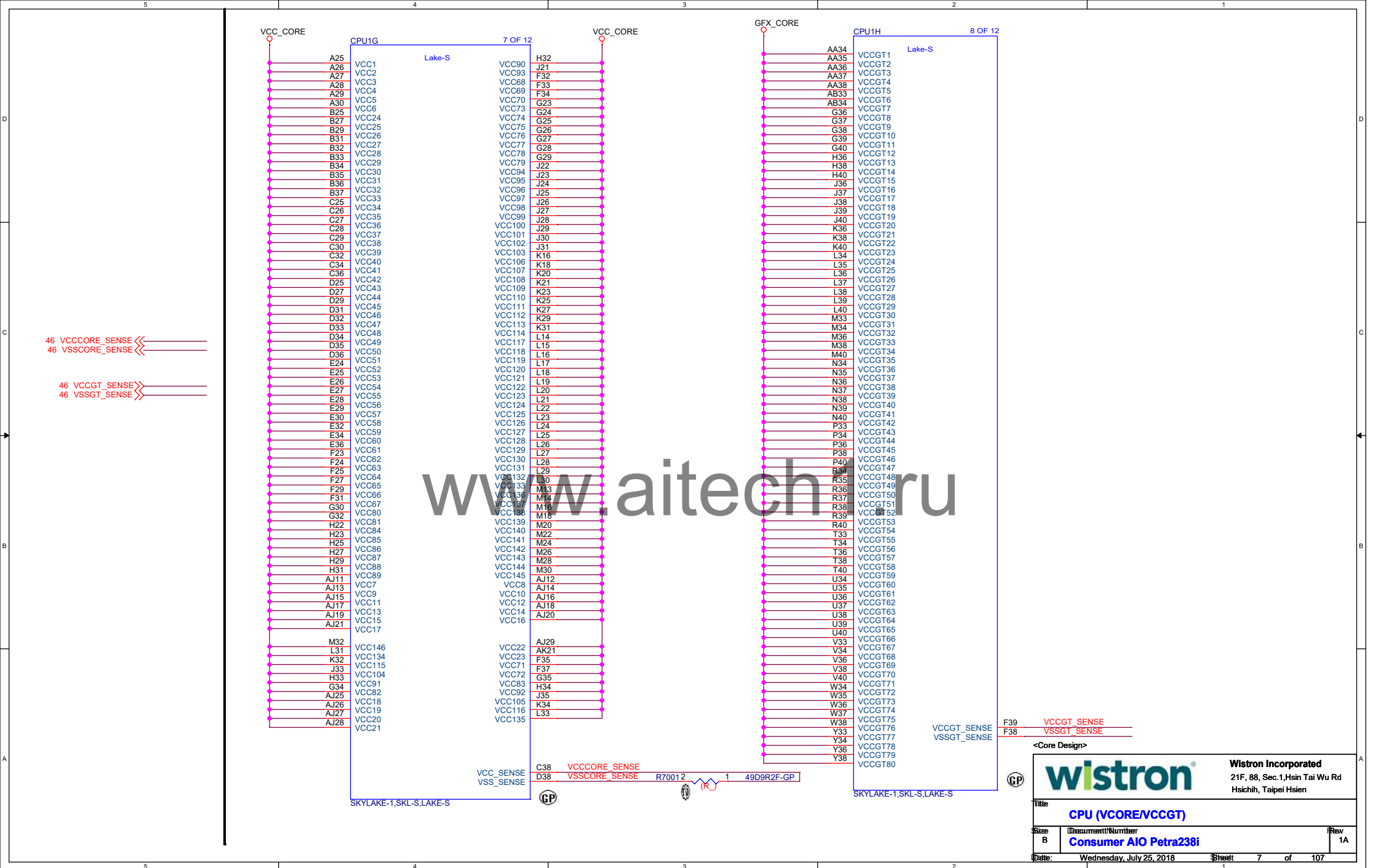
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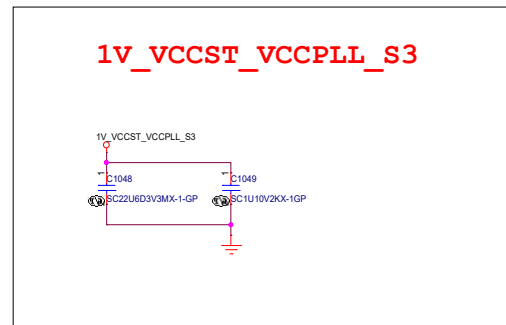
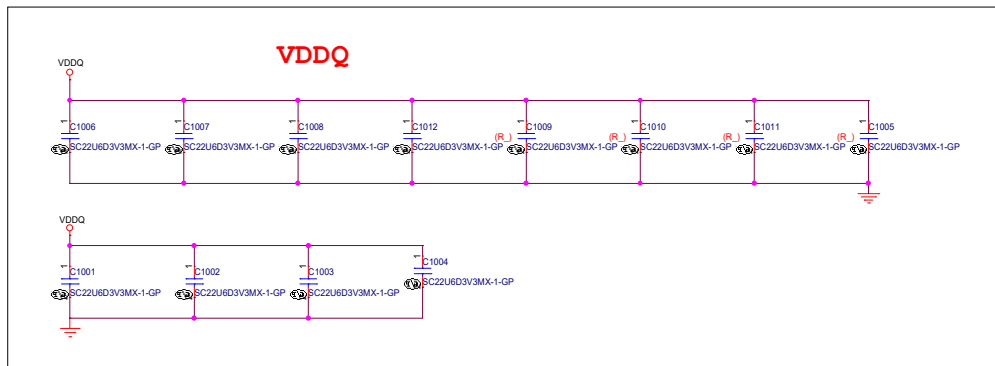
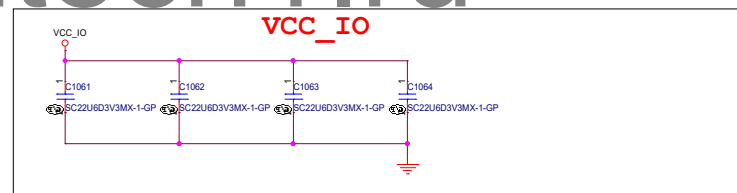
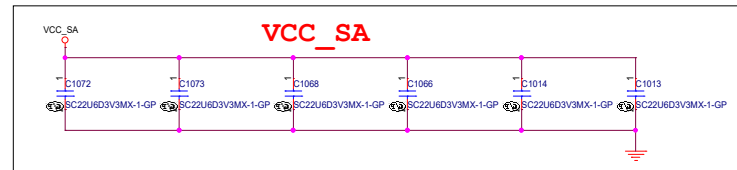
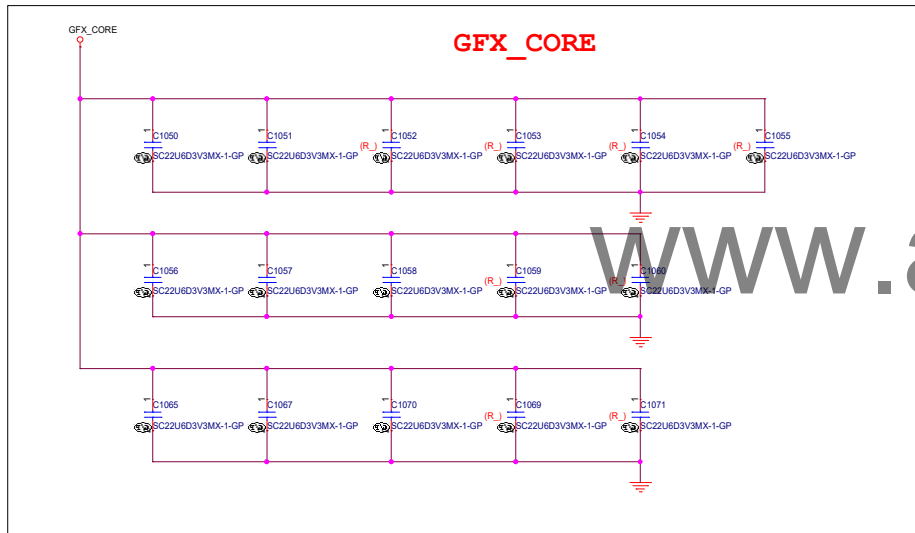
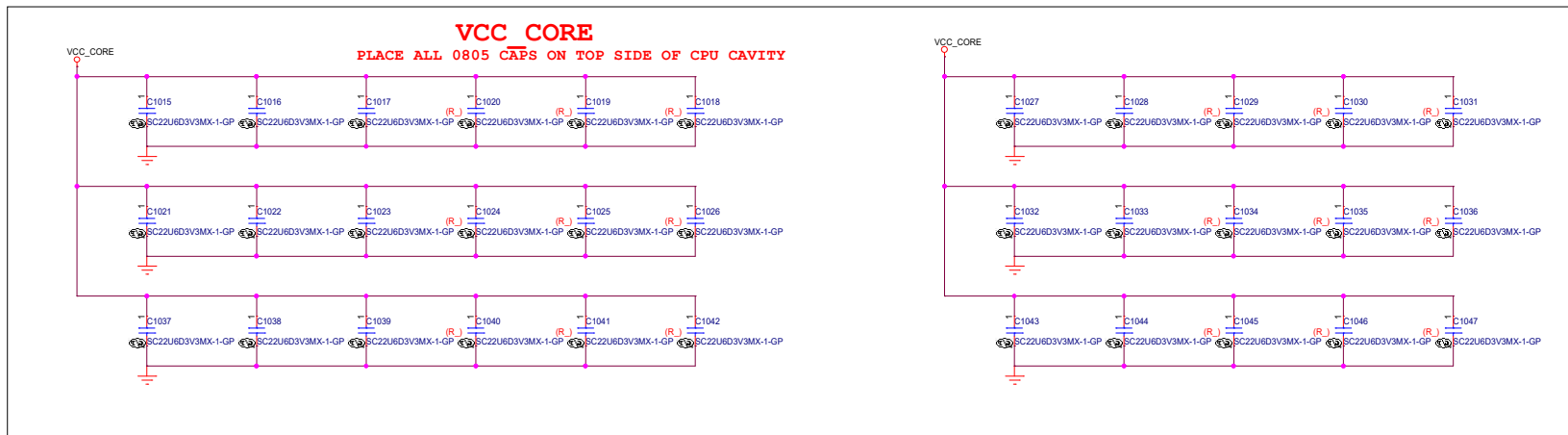
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Hsichih, Taipei Hsien

Title: CPU (SVID/CFG/JTAG/CLK)

Size: B Document Number: Consumer AIO Petra238i Rev: 1A

Date: Wednesday, July 25, 2018 Sheet: 6 of 107




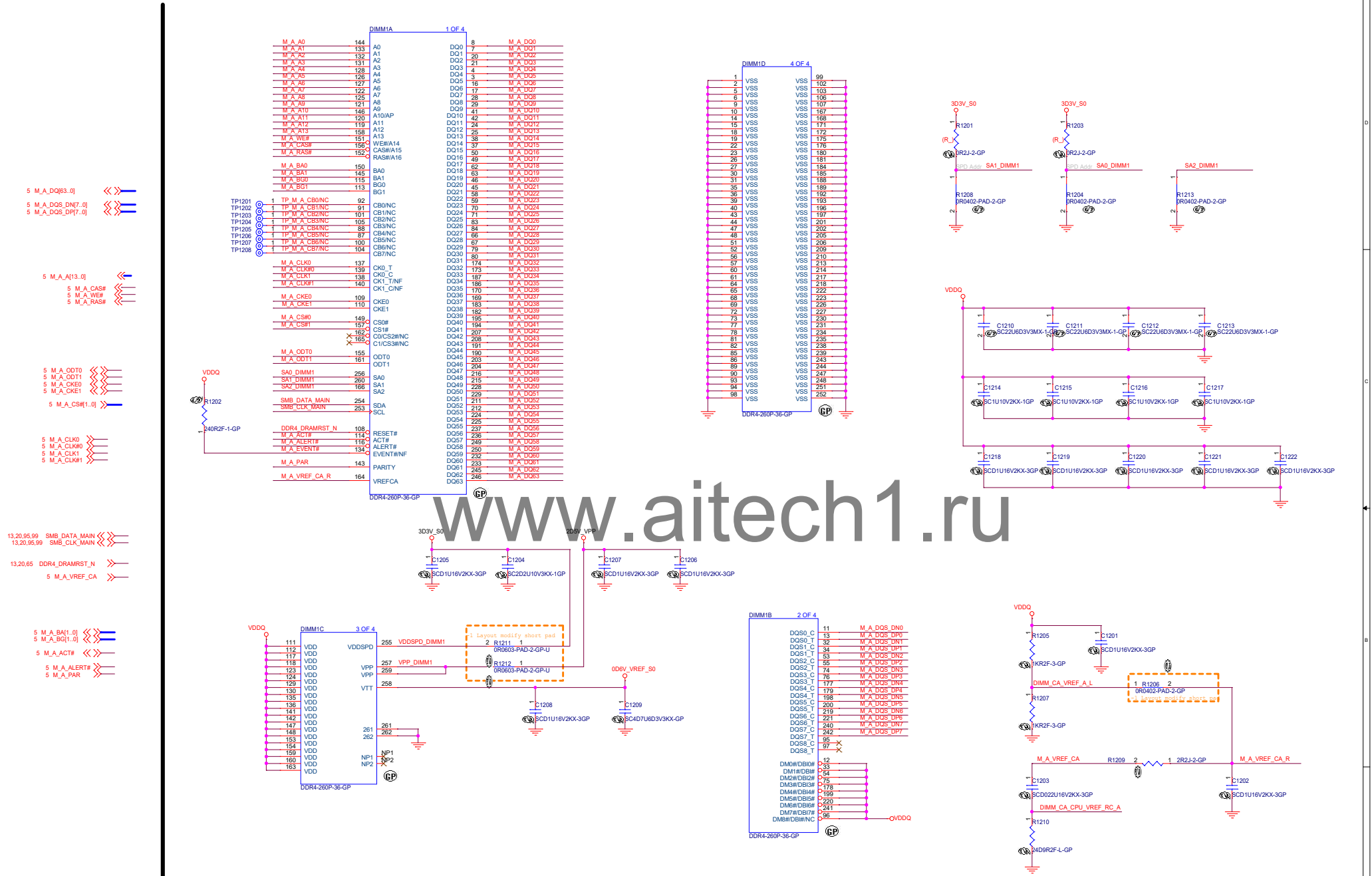


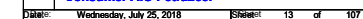
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| Title CPU Power CAP2 | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet | 11 of 107 |

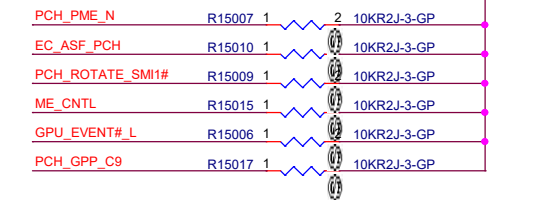


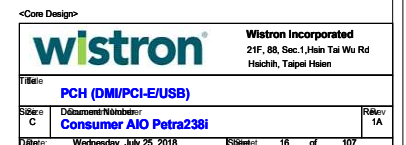


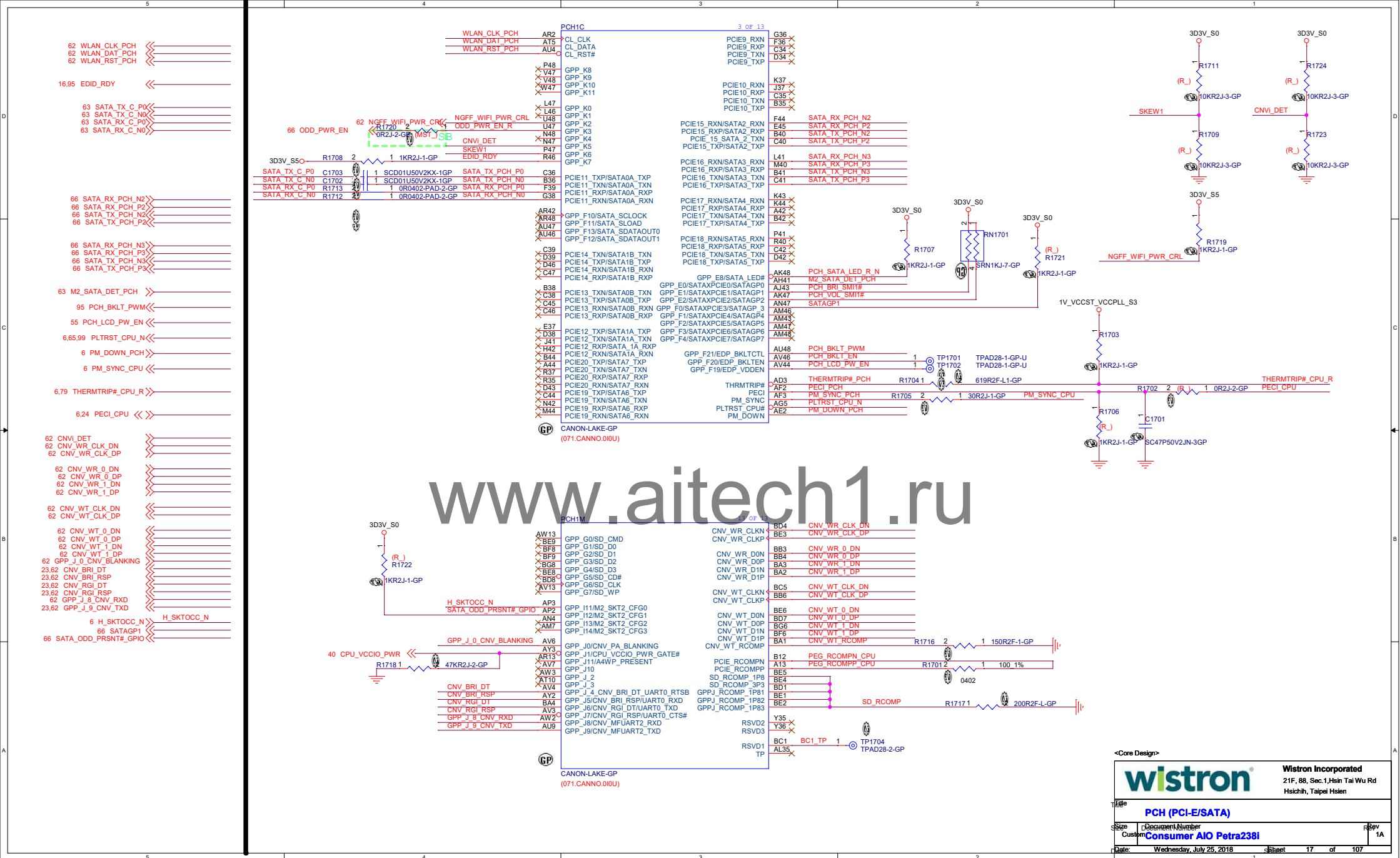
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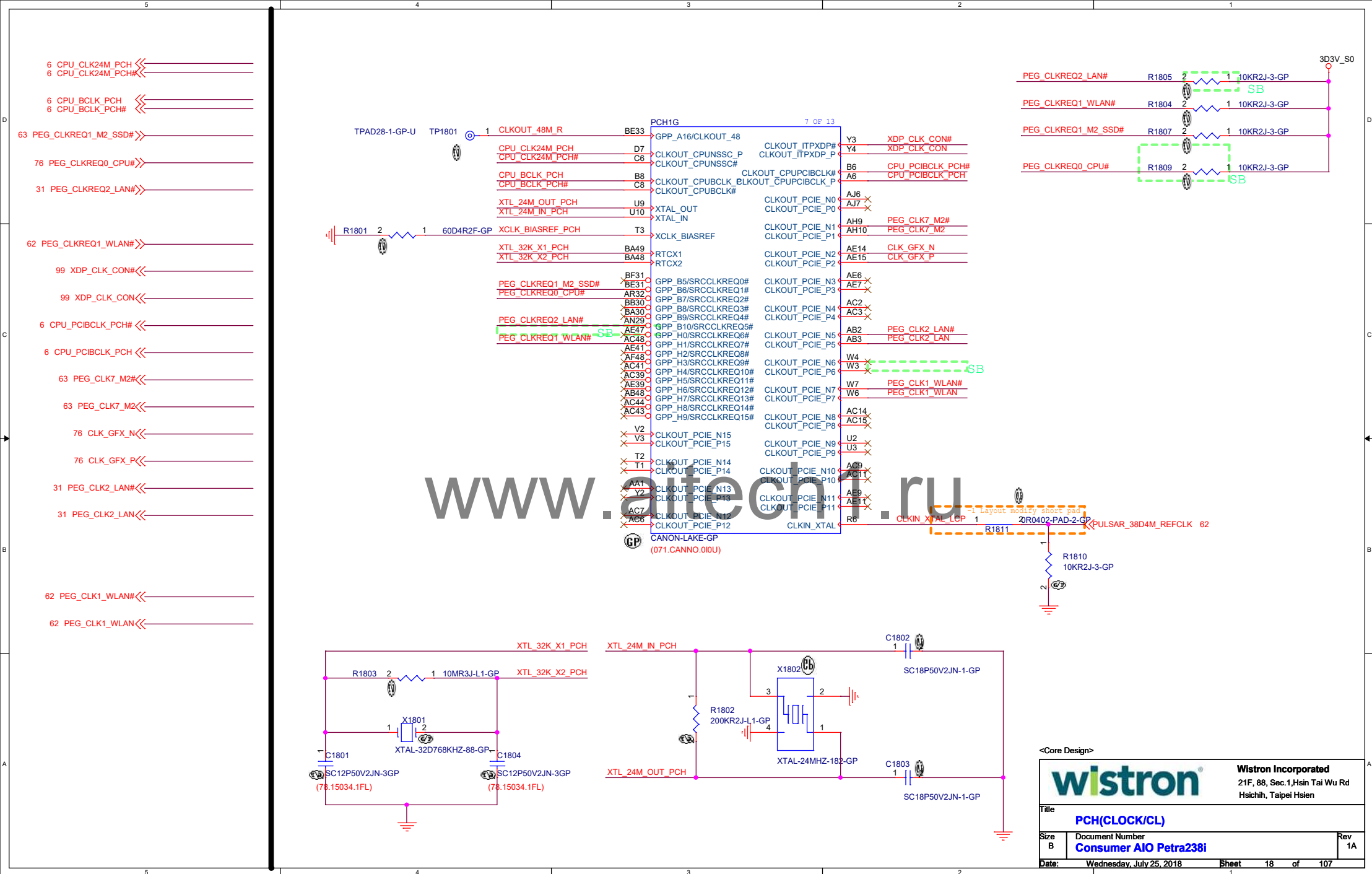
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|  | | Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien | |
| Title DDR (RSVD) (DDR4-CHA1) | | | |
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| Date: | Wednesday, July 25, 2018 | Sheet | 14 of 107 |









34 USB30_TX_R_N1
34 USB30_TX_R_P1
34 USB31_RX_C_N1
34 USB31_RX_C_P1

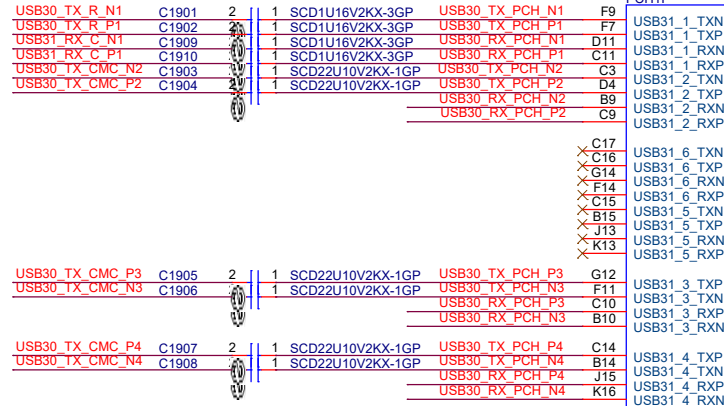
38 USB30_TX_CMC_N2
38 USB30_TX_CMC_P2
38 USB30_RX_PCH_N2
38 USB30_RX_PCH_P2

38 USB30_TX_CMC_P3
38 USB30_TX_CMC_N3
38 USB30_RX_PCH_P3
38 USB30_RX_PCH_N3

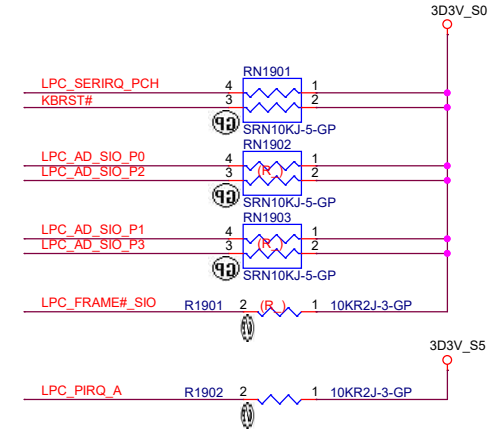
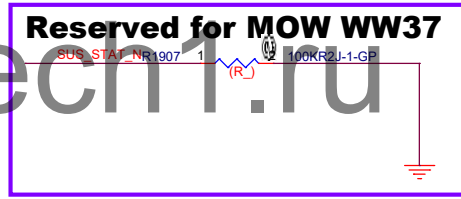
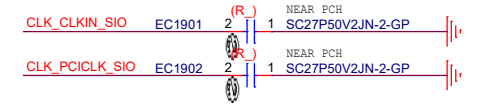
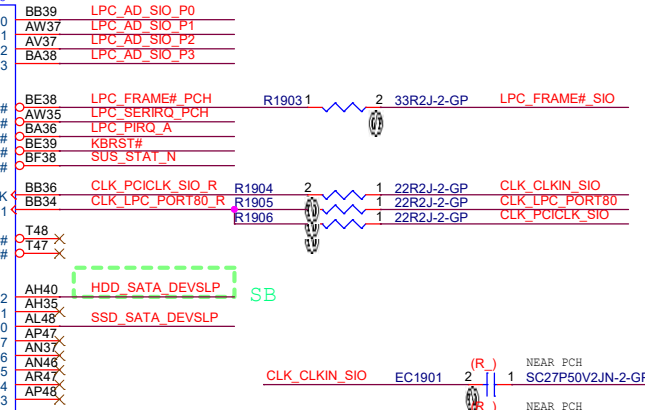
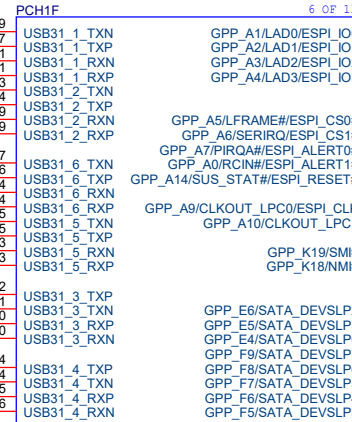
38 USB30_TX_CMC_P4
38 USB30_TX_CMC_N4
38 USB30_RX_PCH_P4
38 USB30_RX_PCH_N4

63 SSD_SATA_DEVS LP
66 HDD_SATA_DEVS LP
24,68 LPC_AD_SIO_P0
24,68 LPC_AD_SIO_P1
24,68 LPC_AD_SIO_P2
24,68 LPC_AD_SIO_P3
24,68 LPC_FRAME#_SIO
24 LPC_SERIRQ_PCH
24 KBRST#

68 CLK_LPC_PORT80
24 CLK_PCICLK_SIO
24 CLK_CLKIN_SIO



CANON-LAKE-GP
(071.CANNO.010U)



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Title
PCH (USB/ESPI)

Size B Document Number
Consumer AIO Petra238i

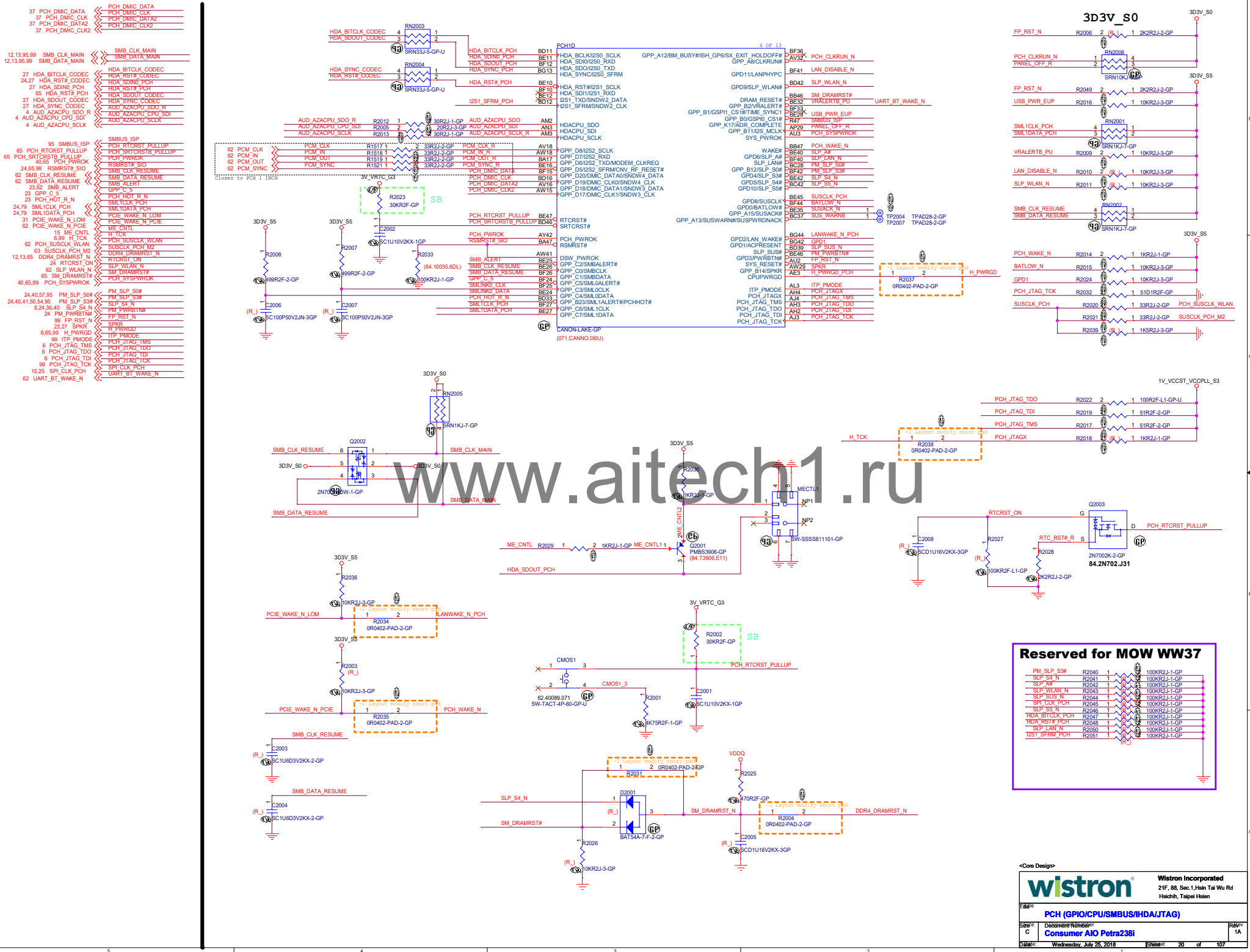
Date: Wednesday, July 25, 2018 Sheet 19 of 107

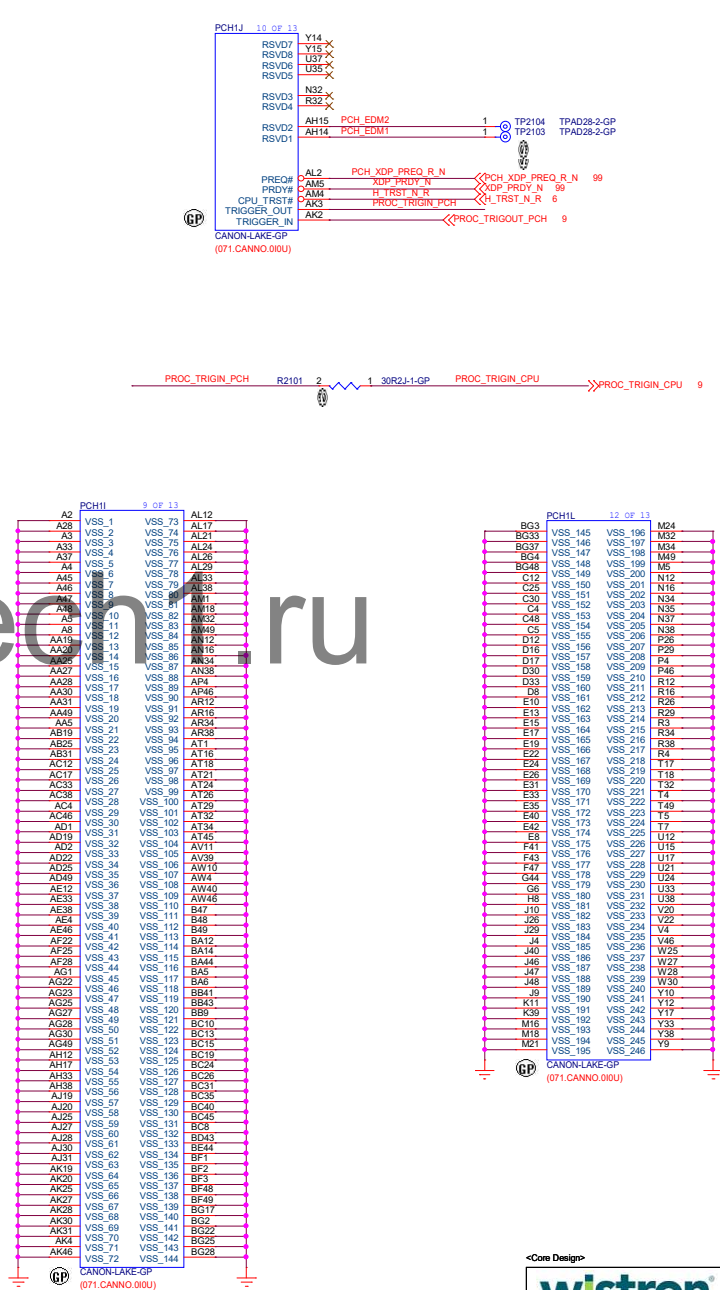
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12,13,95,99 SMB_CLK_MAIN SMB_DATA_MAIN
12,13,95,99 SMB_CLK_MAIN SMB_DATA_MAIN

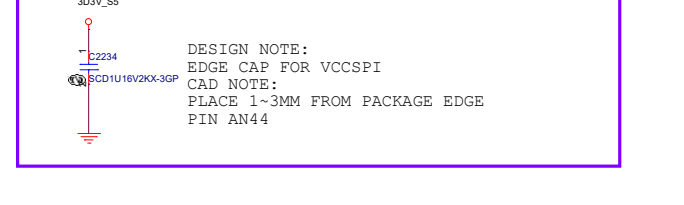
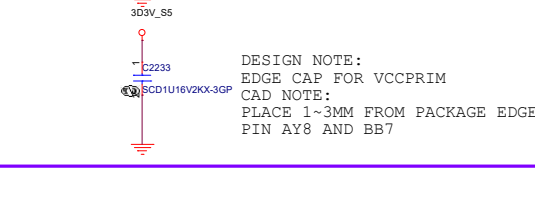
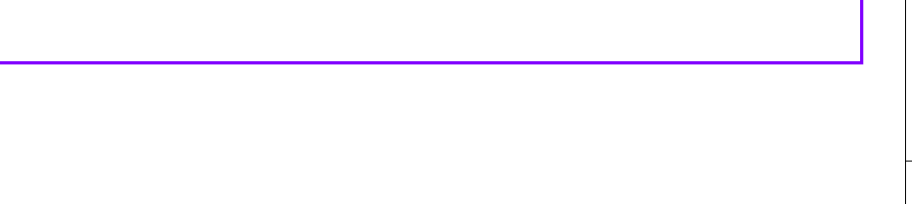
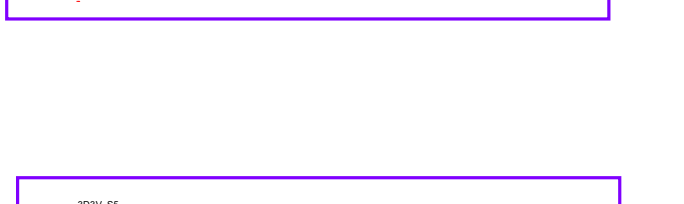
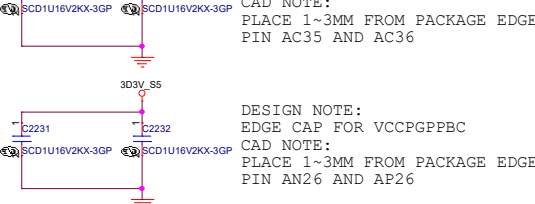
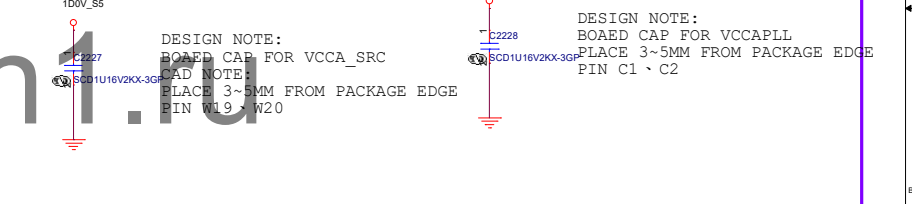
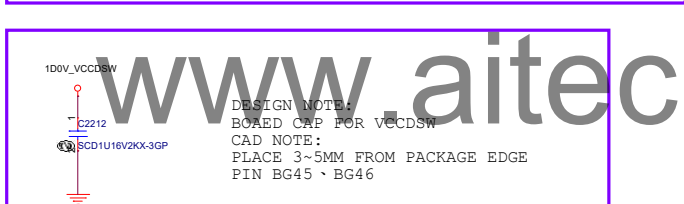
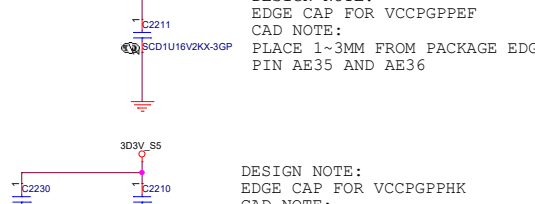
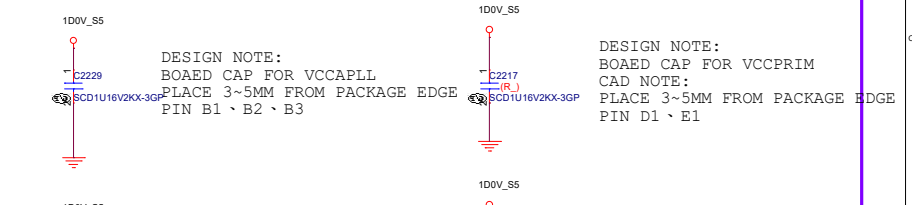
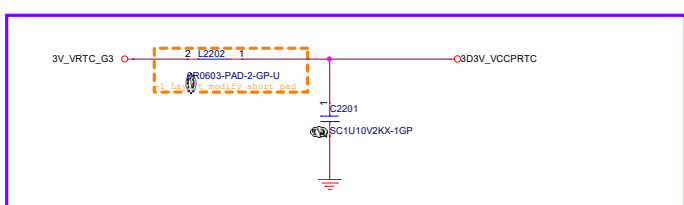
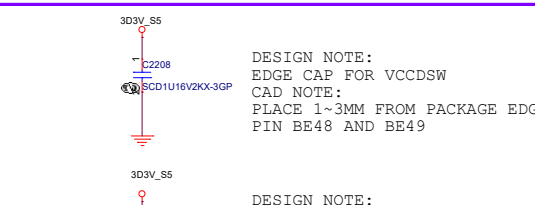
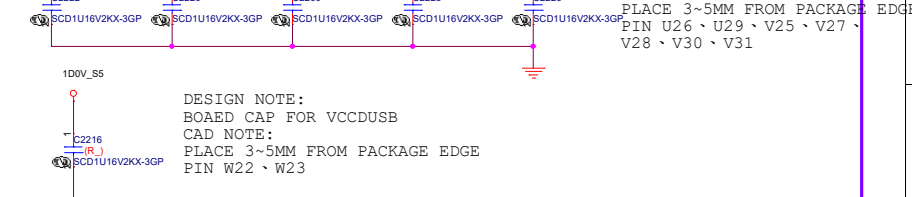
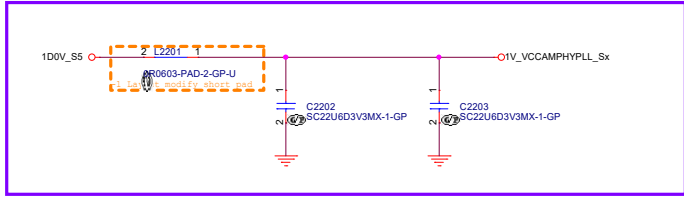
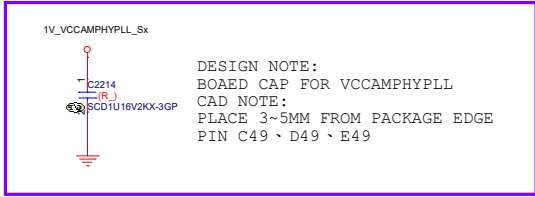
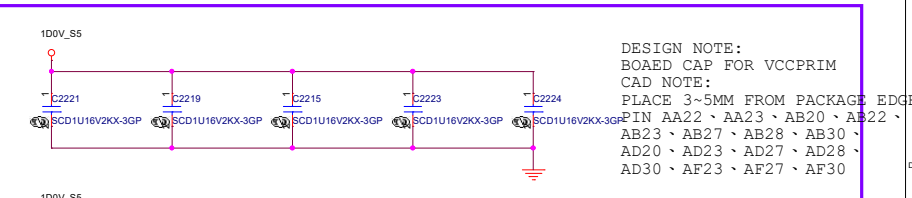
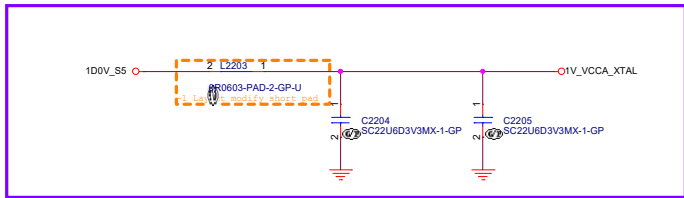
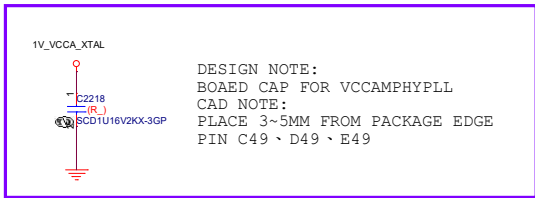
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24,27 HDA_SDOUD_CODECD HDA_SDOUD_CODECD
27 HDA_SDOUD_PCH HDA_SDOUD_PCH
65 HDA_RST#_PCH HDA_RST#_PCH
27 HDA_SDOUD_CODECD HDA_SDOUD_CODECD
27 HDA_SDOUD_PCH HDA_SDOUD_PCH
4 AUD_AZACPU_SDO_R AUD_AZACPU_SDO_R
4 AUD_AZACPU_CPU_SDO AUD_AZACPU_CPU_SDO
4 AUD_AZACPU_SCLK AUD_AZACPU_SCLK

95 SMBUS_ISP SMBUS_ISP
65 PCH_RTICRST_PULLUP PCH_RTICRST_PULLUP
40,65 PCH_PWRROK PCH_PWRROK
24,65,99 RSMRST#_SIO RSMRST#_SIO
62 SMB_CLK_RESUME SMB_CLK_RESUME
62 SMB_DATA_RESUME SMB_DATA_RESUME
23,62 SMB_ALERT SMB_ALERT
23 GPP_C_5 GPP_C_5
23 PCH_HOT_R_N PCH_HOT_R_N
24,79 SML1CLK_PCH SML1CLK_PCH
24,79 SML1DATA_PCH SML1DATA_PCH
31 PCIE_WAKE_N_LOM PCIE_WAKE_N_LOM
62 PCIE_WAKE_N_PCIE PCIE_WAKE_N_PCIE
15 ME_CNTL ME_CNTL
15 H_TCK H_TCK
62 PCH_SUSCLK_WLAN PCH_SUSCLK_WLAN
63 SUSCLK_PCH_M2 SUSCLK_PCH_M2
12,13,65 DDR4_DRAMRST#_N DDR4_DRAMRST#_N
24 RTICRST_ON RTICRST_ON
62 SLP_WLAN_N SLP_WLAN_N
65 SM_DRAMRST# SM_DRAMRST#
40,65,99 PCH_SYSPWRROK PCH_SYSPWRROK

24,40,57,95 PM_SLP_S3# PM_SLP_S3#
24,40,41,50,54,95 PM_SLP_S3# PM_SLP_S3#
8,24,36,40 SLP_S4_N SLP_S4_N
24 PM_PWRBTN# PM_PWRBTN#
99 FP_RST_N FP_RST_N
23,27 SPKR SPKR
6,65,99 H_PWRROK H_PWRROK
99 ITP_PMODE ITP_PMODE
8 PCH_JTAG_TMS PCH_JTAG_TMS
6 PCH_JTAG_TDO PCH_JTAG_TDO
6 PCH_JTAG_TDI PCH_JTAG_TDI
99 PCH_JTAG_TCK PCH_JTAG_TCK
15,25 SPI_CLK_PCH SPI_CLK_PCH
62 UART_BT_WAKE_N UART_BT_WAKE_N









SPI0_MOSI

BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

SPI0_MISO

BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

SPI0_IO2

CONSENT STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

SPI_HOLD_PCH

PERSONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

GPP_B14
SPK_R

TOP SWAP OVERRIDE STRAP
HIGH/LOW SWAP ENABLED
LOW/NO SWAP (DISABLED/DEFAULT)
PCH HAS INTERNAL WEAK PU

GPP_B18
GSP10_MOSI

NO REBOOT IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PU

GPP_C2
SMB_ALERT#

TLS CONFIDENTIALITY ENABLED
IF SAMPLED HIGH (DEFAULT)
PCH HAS INTERNAL WEAK PU

GPP_B22
GSP11_MOSI

BOOT HALT STRAP
IF SAMPLED HIGH, LPC IS REBOOTED
THIS IS A LOW/NO PU ON THE M7
PCH HAS INTERNAL WEAK PU

GPP_C5
SMO_ALERT#

SWP/LPC SELECT STRAP
IF SAMPLED HIGH, SWP IS SELECTED ELSE LPC
PCH HAS INTERNAL WEAK PU

GPP_B23
SML1_ALERT#
PCH_HOT#

This signal has an internal pull-down.
0 = Disable Intel® DCI-OOB (Default)
1 = Enable Intel® DCI-OOB

GPP_H12
SML2_ALERT#
GPP_H15
SML3_ALERT#

ESPI FLASH SHARING MODE
0: MASTER ATTACHED FLASH SHARING
1: SLAVE ATTACHED FLASH SHARING
PCH HAS INTERNAL WEAK PU
Note: This signal is connected to the ESPI flash sharing mode strap. The strap must be configured to '0' (ESPI is disabled) if the ESPI flash sharing mode strap is configured to '0' (ESPI is disabled).
Note: If the ESPI flash sharing mode strap is configured to '1' (ESPI is enabled), the ESPI flash sharing mode strap must be configured to '0' (ESPI is disabled).
Note: If the ESPI flash sharing mode strap is configured to '1' (ESPI is enabled), the ESPI flash sharing mode strap must be configured to '0' (ESPI is disabled).

GPP_I6
DDP_C_CTRLDATA
GPP_I8
DDP_C_CTRLDATA
GPP_I10
DDP_D_CTRLDATA

ESPI FLASH SHARING MODE
0: MASTER ATTACHED FLASH SHARING
1: SLAVE ATTACHED FLASH SHARING
PCH HAS INTERNAL WEAK PU
Note: This signal is connected to the ESPI flash sharing mode strap. The strap must be configured to '0' (ESPI is disabled) if the ESPI flash sharing mode strap is configured to '0' (ESPI is disabled).
Note: If the ESPI flash sharing mode strap is configured to '1' (ESPI is enabled), the ESPI flash sharing mode strap must be configured to '0' (ESPI is disabled).
Note: If the ESPI flash sharing mode strap is configured to '1' (ESPI is enabled), the ESPI flash sharing mode strap must be configured to '0' (ESPI is disabled).

GPP_F23

GP07 connects to CNV_BRI and is used as GPP_BRI_RSP.

HDA_SDO
I2S0_TXD

GPP_H17
DPP_C_CTRLDATA

GPP_H_17 is muxed with SML4_DATA and not DDP_C_CTRLDATA.
GPP_H_17 is not a PCH strap in the latest CNV-H pinlist description.

GPP_J4
CNV_BRI_DT
UART0_RTS#

GPP_J6
CNV_RGI_DT
UART0_TXD

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

GPP_J9

The signal has a weak internal pull-down.
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

GP07

XTAL INPUT MODE
HIGH: XTAL INPUT IS DIFFERENTIAL
LOW: XTAL INPUT IS SINGLE-ENDED
PCH HAS INTERNAL 20K PU

HDA_SDO
I2S0_TXD

ME disable

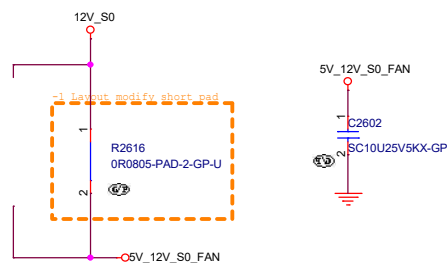
| Signal | Usage | When Sampled | Comment |
|----------------------|---------------------|--------------------------|---|
| GPP_B14 / SPKR | Top Swap Override | Rising edge of FCH_PWR0K | The signal has a weak internal Pull-down. 0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the PCH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap. Notes: 1. The internal Pull-down is disabled after PCH_PWR0K is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (BusD, Device3), Function0, offset DCH, bit4. 4. This signal is in the primary well. |
| GPP_B18 / GSP10_MOSI | No Reboot | Rising edge of FCH_PWR0K | The signal has a weak internal Pull-down. 0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode. PCH will disable the TCS timer system related features. This function is useful when running IT/VSOP. Notes: 1. The internal Pull-down is disabled after PCH_PWR0K is high. 2. This signal is in the primary well. |
| GPP_C2 / SMBALERT# | TLS Confidentiality | Rising edge of FCH_PWR0K | This signal has a weak internal Pull-down. 0 = Disable Intel® M7 Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel® M7 Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. Notes: 1. The internal Pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. |

| Signal | Usage | When Sampled | Comment |
|----------------------------------|----------------------|--------------------------|--|
| GPP_B22 / GSP11_MOSI | Boot BIOS Strap BIOS | Rising edge of FCH_PWR0K | This signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (BusD, Device3), Function0, offset DCH, bit 0. BIOS 0 SPI (Default) 1 LPC Notes: 1. The internal pull-down is disabled after FCH_PWR0K is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated QLE LAN. 4. This signal is in the primary well. |
| GPP_C5 / SML3_ALERT# | eSPI or LPC | Rising edge of RSMRST# | This signal has a weak internal pull-down. 0 = LPC is selected (for EC). (Default) 1 = eSPI is selected (for EC). Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. Warning: If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' (eSPI is disabled). |
| SPI0_MOSI | Reserved | Rising edge of RSMRST# | External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |
| GPP_H15 / SML3_ALERT# | Reserved | Rising edge of RSMRST# | External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |
| GPP_B23 / SML1_ALERT# / PCH_HOT# | Intel® DCI-OOB | Rising edge of RSMRST# | This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCH_HOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. |
| SPI0_IO2 | Reserved | Rising edge of RSMRST# | External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |

| Signal | Usage | When Sampled | Comment |
|--------------------------|------------------------------------|--------------------------|--|
| SPI0_IO3 | Reserved | Rising edge of RSMRST# | External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |
| HDA_SDO / I2S0_TXD | Flash Descriptor Security Override | Rising edge of FCH_PWR0K | 0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (overrides). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. Notes: 1. The internal pull-down is disabled after FCH_PWR0K is high. 2. This signal is in the primary well. This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled). |
| GPP_H12 / SML2_ALERT# | eSPI Flash Sharing Mode | Rising edge of RSMRST# | This signal has a weak internal pull-down. 0 = Port B is detected. (Default) 1 = Port F is detected. Notes: 1. The internal pull-down is disabled after FCH_PWR0K de-asserts. 2. This signal is in the primary well. |
| GPP_I6 / DDP_C_CTRLDATA | Display Port D Detected | Rising edge of FCH_PWR0K | This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port F is not detected. (Default) Notes: 1. The internal pull-down is disabled after FCH_PWR0K de-asserts. 2. This signal is in the primary well. |
| GPP_I8 / DDP_C_CTRLDATA | Display Port C Detected | Rising edge of FCH_PWR0K | This signal has a weak internal pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. Notes: 1. The internal pull-down is disabled after FCH_PWR0K de-asserts. 2. This signal is in the primary well. |
| GPP_I10 / DDP_D_CTRLDATA | Display Port D Detected | Rising edge of FCH_PWR0K | This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. Notes: 1. The internal pull-down is disabled after FCH_PWR0K de-asserts. 2. This signal is in the primary well. |
| GPP_F23 | Display Port F Detected | Rising edge of FCH_PWR0K | This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. Notes: 1. The internal pull-down is disabled after FCH_PWR0K de-asserts. 2. This signal is in the primary well. |

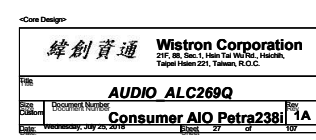
| Signal | Usage | When Sampled | Comment |
|----------------------------------|-----------------------|--------------------------|---|
| GPP_J4 / CNV_BRI_DT / UART0_RTS# | XTAL Frequency Select | Rising edge of RSMRST# | This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 MHz XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. |
| GPP_J6 / CNV_RGI_DT / UART0_TXD | M.2 CNV Mode Select | Rising edge of RSMRST# | An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable. |
| GPP_J9 | 1.8V VCCSPI | Rising edge of RSMRST# | The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os. |
| GP07 | Reserved | Rising edge of FCH_PWR0K | External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |





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| Title | | | |
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| Size | Document Number | | Rev |
| Custom | Consumer AIO Petra238i | | 1 |
| Date | Wednesday, July 25, 2018 | Sheet | 26 of 107 |



27.85 I2S_OUT_R
27.85 I2S_OUT_L
27.85 I2S_MCLK_R
27.85 I2S_MCLK_L

25 SPKR_OUT_L+
25 SPKR_OUT_L-
25 SPKR_OUT_R+
25 SPKR_OUT_R-

Scalar

95 AMP_DOUT
95 AMP_SCLK
95 AMP_LRCLK
95 AMP_MCK

25.95 SCALAR_AMP_MUTE
27.25.95 PC_MONITOR_SW

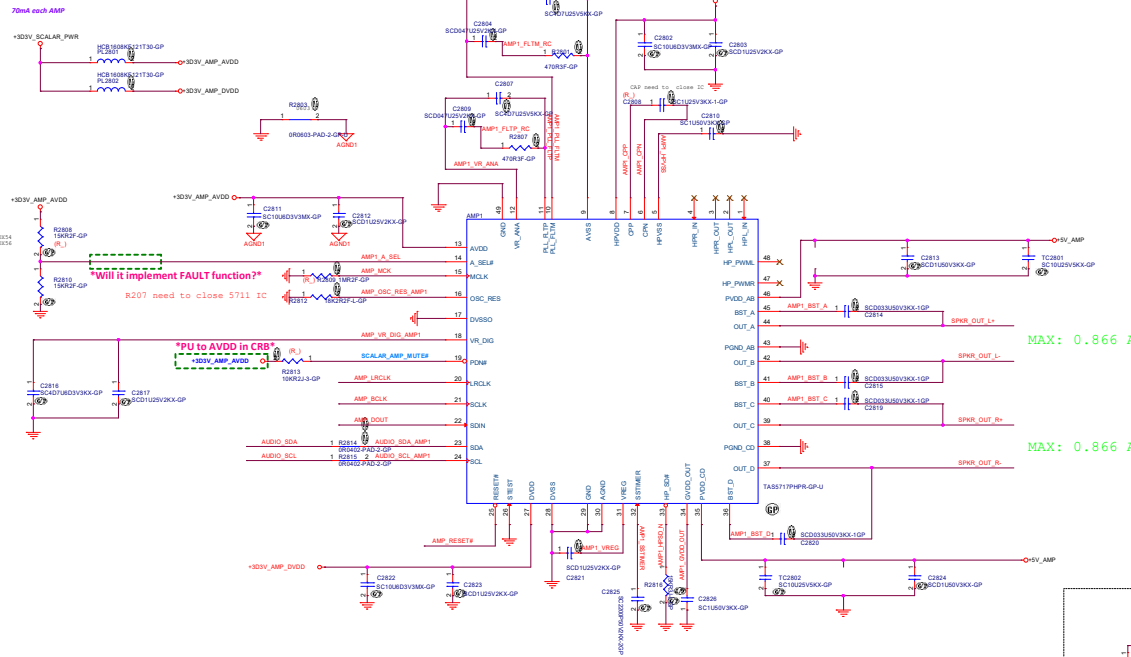
95 AUDIO_SCL
95 AUDIO_SDA

Scalar HP LINE OUT

97.85 SCALAR_HP_OUT_R+
97.85 SCALAR_HP_OUT_L+
97.85 SCALAR_HP_OUT_R-
97.85 SCALAR_HP_OUT_L-

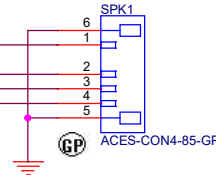
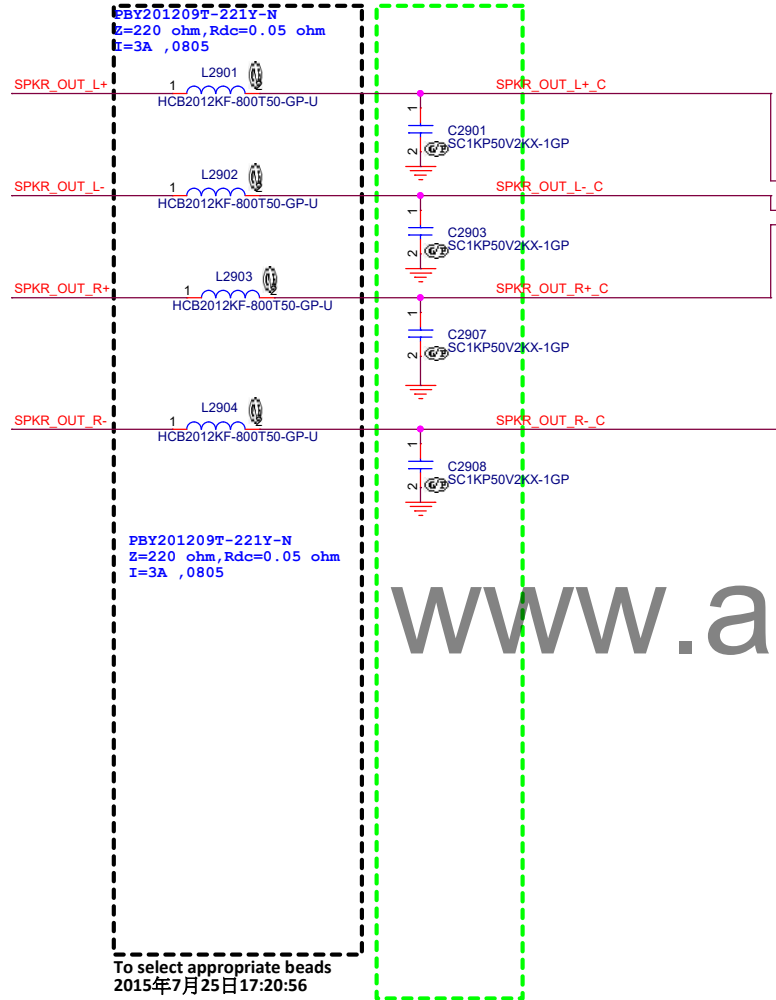
Control

27.25.95 PC_MONITOR_SW

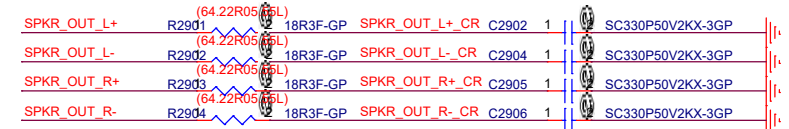
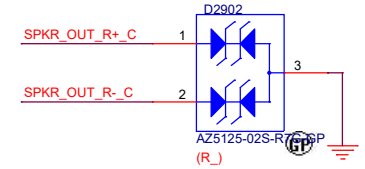
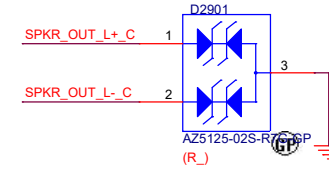


28 SPKR_OUT_L+
28 SPKR_OUT_L-
28 SPKR_OUT_R+
28 SPKR_OUT_R-

LC need to
close AMP IC



Need to check Pin define



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<Variant Name>

wistron

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12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

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Audio Speak&Woofers

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Date: Wednesday, July 25, 2018

Document Number
Petar238i

Rev
SA

Sheet 29 of 107

RSVD

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<Variant Name>

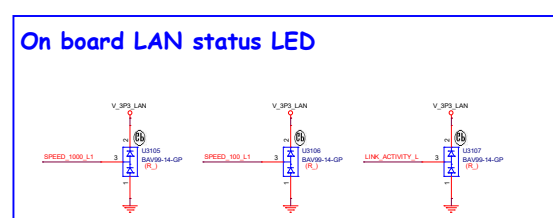
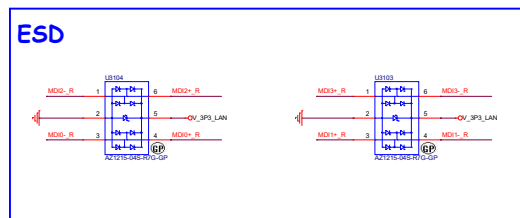
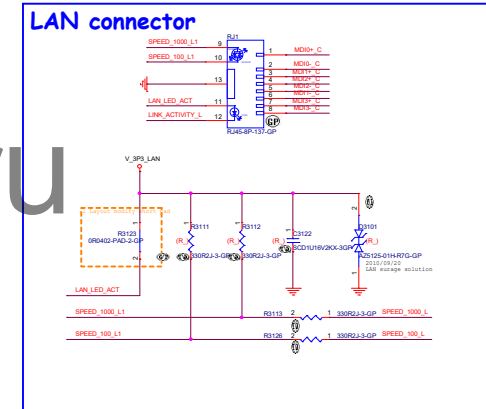
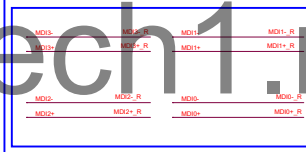
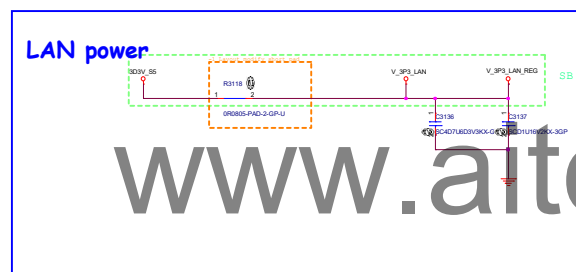
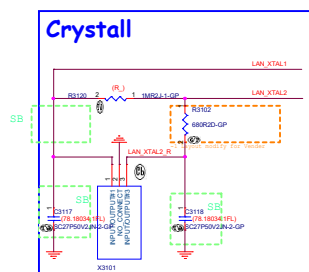
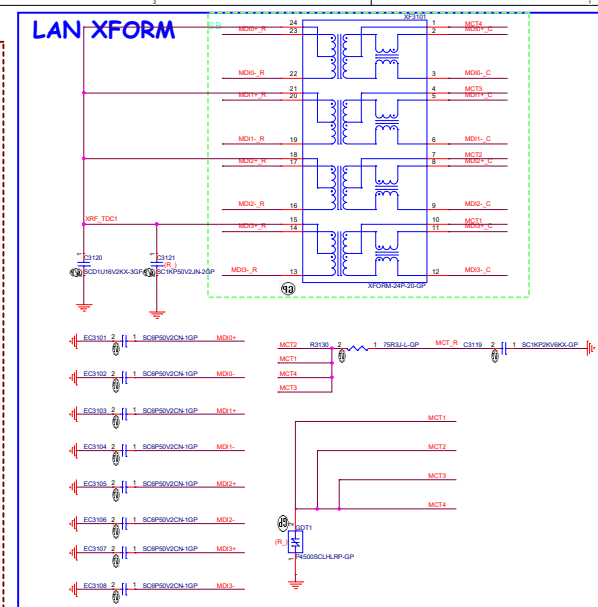
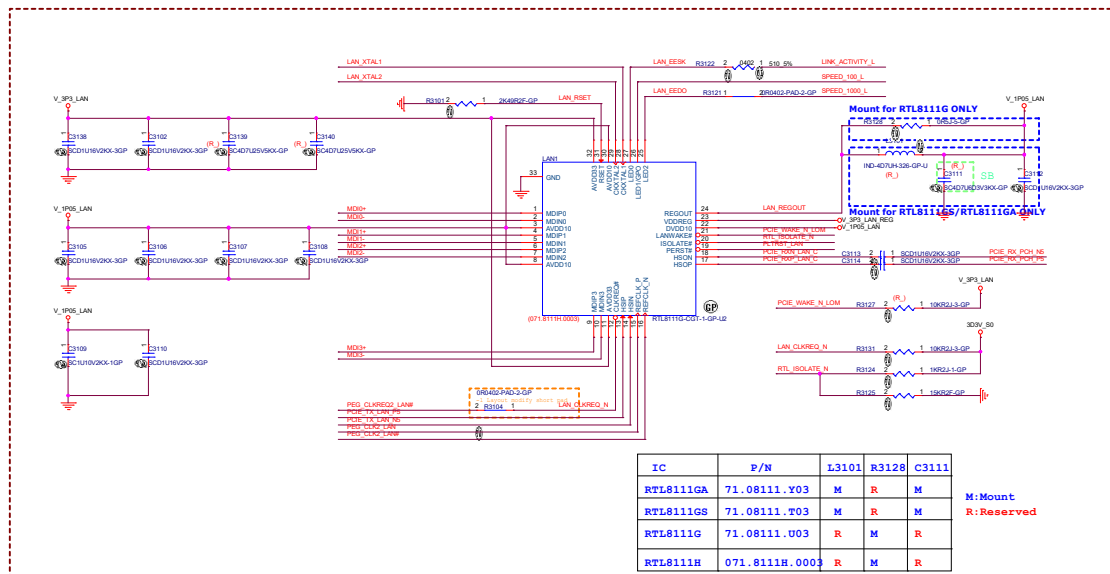
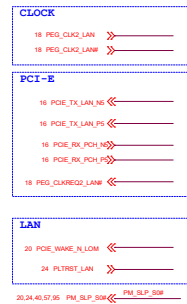
wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
Audio Speak&Woofers

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| Size B | Document Number Consumer AIO Petra238i | Rev 1A |
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|-------|--------------------------|-------|----|----|-----|
| Date: | Wednesday, July 25, 2018 | Sheet | 30 | of | 105 |
|-------|--------------------------|-------|----|----|-----|



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|  | | Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien | |
| Title RJ45&Transformer | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet | 32 of 107 |

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| <Core Design> | | | |
|  | | Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Haichih, Taipei Hsien | |
| Title Card reader BH611FJ1LN | | | |
| Size C | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date | Wednesday, Jul 25, 2018 | | Sheet 33 of 107 |

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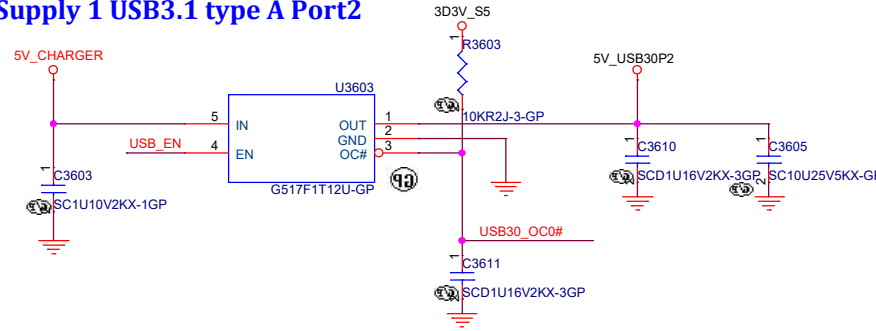
USB over current signal

16 USB30_OC0#
16,36 USB30_OC1#

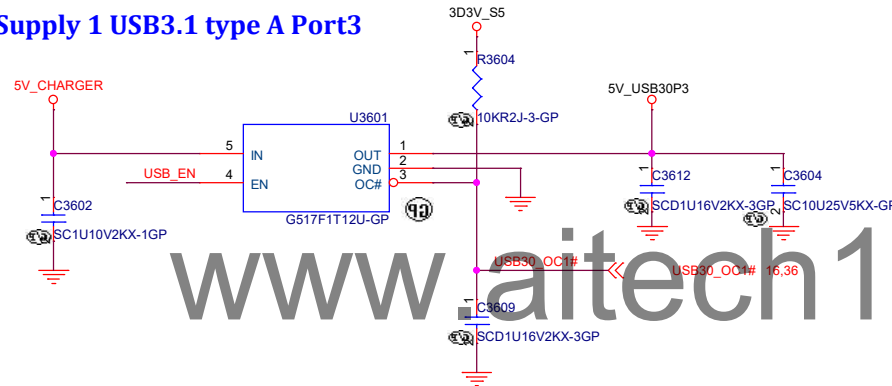
USB power control signal

8,20,24,40 SLP_S4_N
24 EC_USB_POWER_EN
34 USB_EN

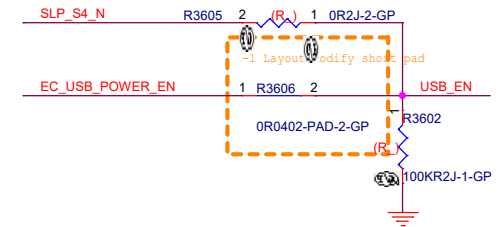
Supply 1 USB3.1 type A Port2



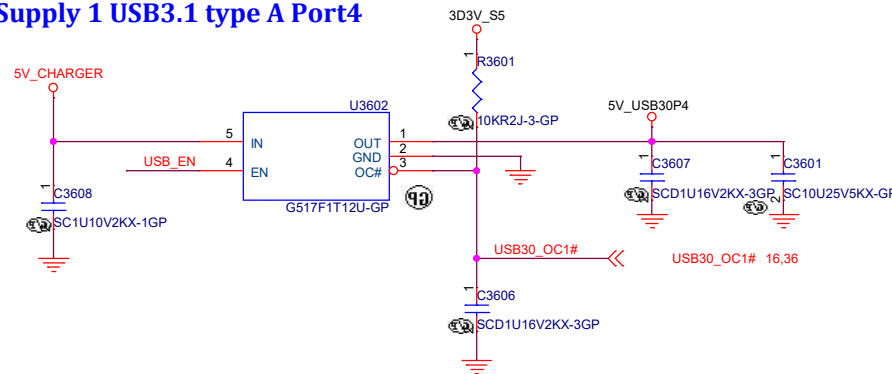
Supply 1 USB3.1 type A Port3



USB3.1 Power control



Supply 1 USB3.1 type A Port4



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Title
Switch power

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Sheet 36 of 107

Rev 1A

USB Port8 -> WEBCAM

USB signal for WEBCAM

16 USB_PCH_PP8
16 USB_PCH_PN8

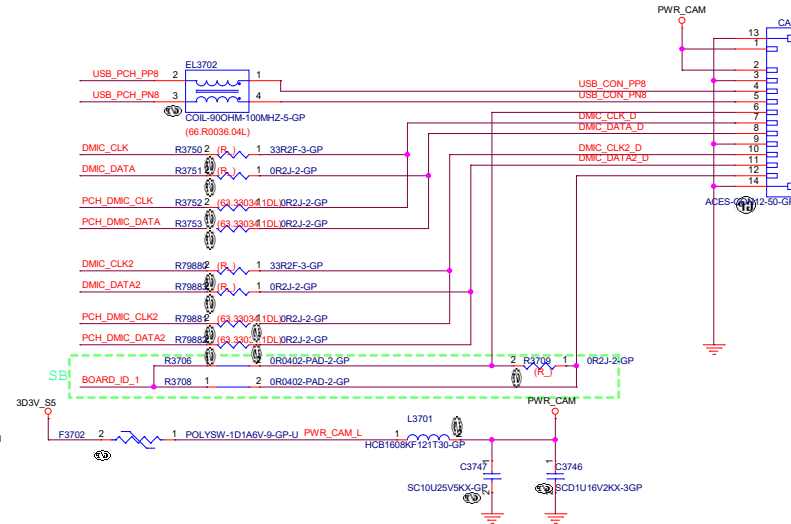
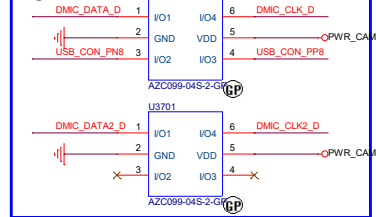
Audiod codec DMIC

27 DMIC_DATA
27 DMIC_CLK
27 DMIC_DATA2
27 DMIC_CLK2

PCH DMIC

20 PCH_DMIC_CLK
20 PCH_DMIC_DATA
20 PCH_DMIC_CLK2
20 PCH_DMIC_DATA2
16 BOARD_ID_1

ESD



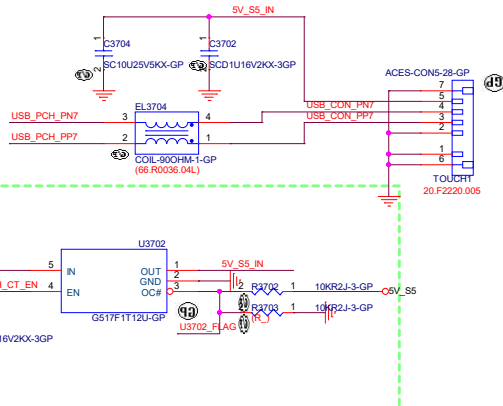
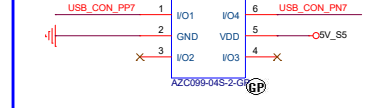
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USB Port7 -> Touch

USB signal for Touch

16 USB_PCH_PP7
16 USB_PCH_PN7

ESD



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File
USB20_FRONT HEADER

Size
Customer
Consumer AIO Petra238i

Date
Wednesday, July 25, 2018

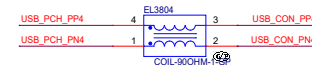
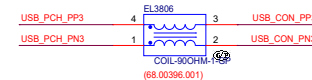
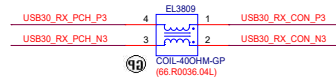
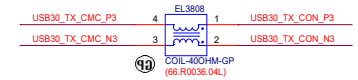
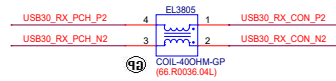
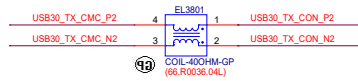
Sheet 37 of 107

USB 3.1 signal

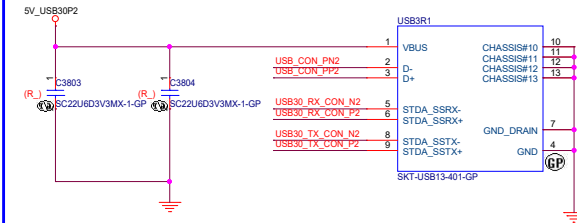
19 USB30_RX_PCH_N2 <<
 19 USB30_RX_PCH_P2 <<
 19 USB30_TX_CMC_N2 >>
 19 USB30_TX_CMC_P2 >>
 19 USB30_RX_PCH_N3 <<
 19 USB30_RX_PCH_P3 <<
 19 USB30_TX_CMC_N3 >>
 19 USB30_TX_CMC_P3 >>
 19 USB30_TX_CMC_N4 <<
 19 USB30_TX_CMC_P4 <<
 19 USB30_RX_PCH_N4 >>
 19 USB30_RX_PCH_P4 >>

USB 2.0 signal

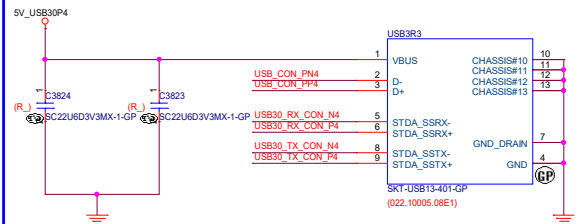
16 USB_PCH_PP2 <<
 16 USB_PCH_PN2 <<
 16 USB_PCH_PP3 <<
 16 USB_PCH_PN3 <<
 16 USB_PCH_PP4 <<
 16 USB_PCH_PN4 <<



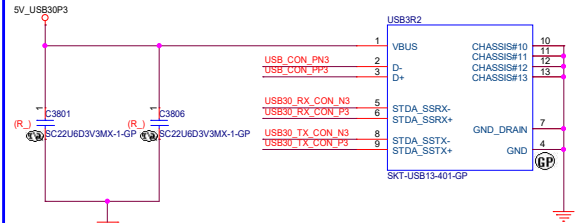
USB3.1 REAR PORT1



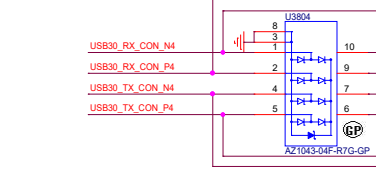
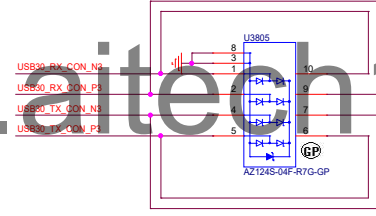
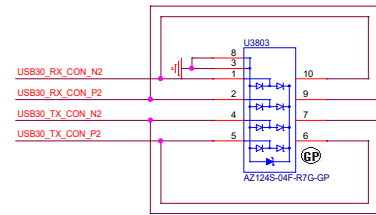
USB3.1 REAR PORT3



USB3.1 REAR PORT2



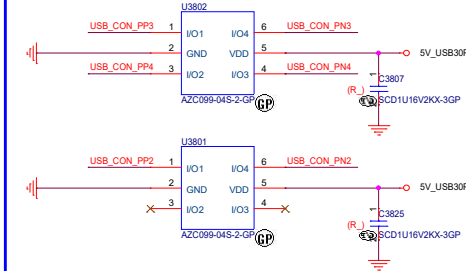
ESD



USB 3.0 Connector Pin definition

| | |
|---|--------------------------|
| 1 | POWER |
| 2 | USB 2.0 D- |
| 3 | USB 2.0 D+ |
| 4 | GND |
| 5 | StdA_SSRX- SuperSpeed RX |
| 6 | StdA_SSRX+ SuperSpeed RX |
| 7 | GND |
| 8 | StdA_SSTX- SuperSpeed TX |
| 9 | StdA_SSTX+ SuperSpeed TX |

ESD



Reserved
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<Core Design>

| | | | |
|---|--|---|-----------|
|  | | Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien | |
| Title USB30_(R) | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet | 39 of 107 |

20,24,40,50,54,95 PM_SLP_S3# >>_____

17,40 CPU_VCCIO_PWR >>_____

20,24,40,57,95 PM_SLP_S0# >>_____



24,66 CTRL0_EUP>>




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21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Date: Wednesday, July 25, 2018 Sheet 41 of 107

RSVD

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<Core Design>



Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title

RSVD

| | | |
|-----------|--|-----------|
| Size B | Document Number Consumer AIO Petra238i | Rev 1A |
|-----------|--|-----------|

| | | | | | |
|-------|--------------------------|-------|----|----|-----|
| Date: | Wednesday, July 25, 2018 | Sheet | 42 | of | 107 |
|-------|--------------------------|-------|----|----|-----|

ANNIE solution

DC-JACK361-GP
022.10015.0481

DCIN1

AD_IK_S

PC8614
SC10U25V5KX-GP

PC4301
SCD1U25V2KX-GP

PC4301
SCD1U50V3KX-GP

PC5MB27A-GP
83 P5MB JAG

DCBATOUT switch

The schematic diagram illustrates the DCBATOUT switch circuit. The input AD_IK_S_R is connected to a network of resistors (R4317, R4318, R4319, R4320) and capacitors (C4309, C4308). The central component is PU4301 (AQ4407-L-GP), which is connected to a power supply PWR_AD*_2 (84.04407, G37). The output is DCBATOUT, which is also connected to a network of resistors and capacitors (R4319, R4320, C4308, C4309).



RSVD

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<Core Design>

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Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title

OZ554A LED Converter

Size

Customer

Document Number

Consumer AIO Petra238i

Date

Wednesday, July 25, 2018

Rev

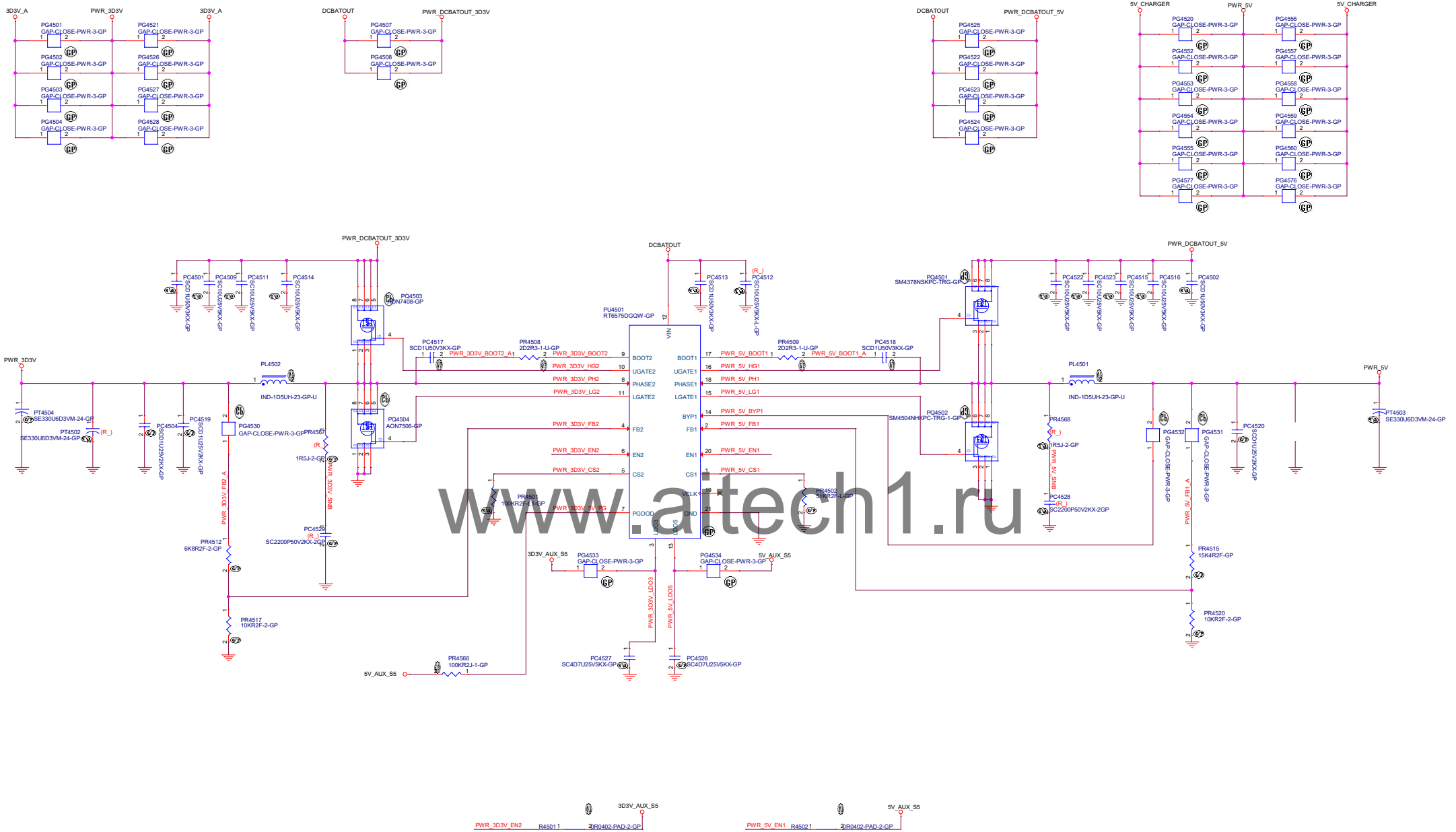
1A

Sheet

44

of

107



<Core Design>

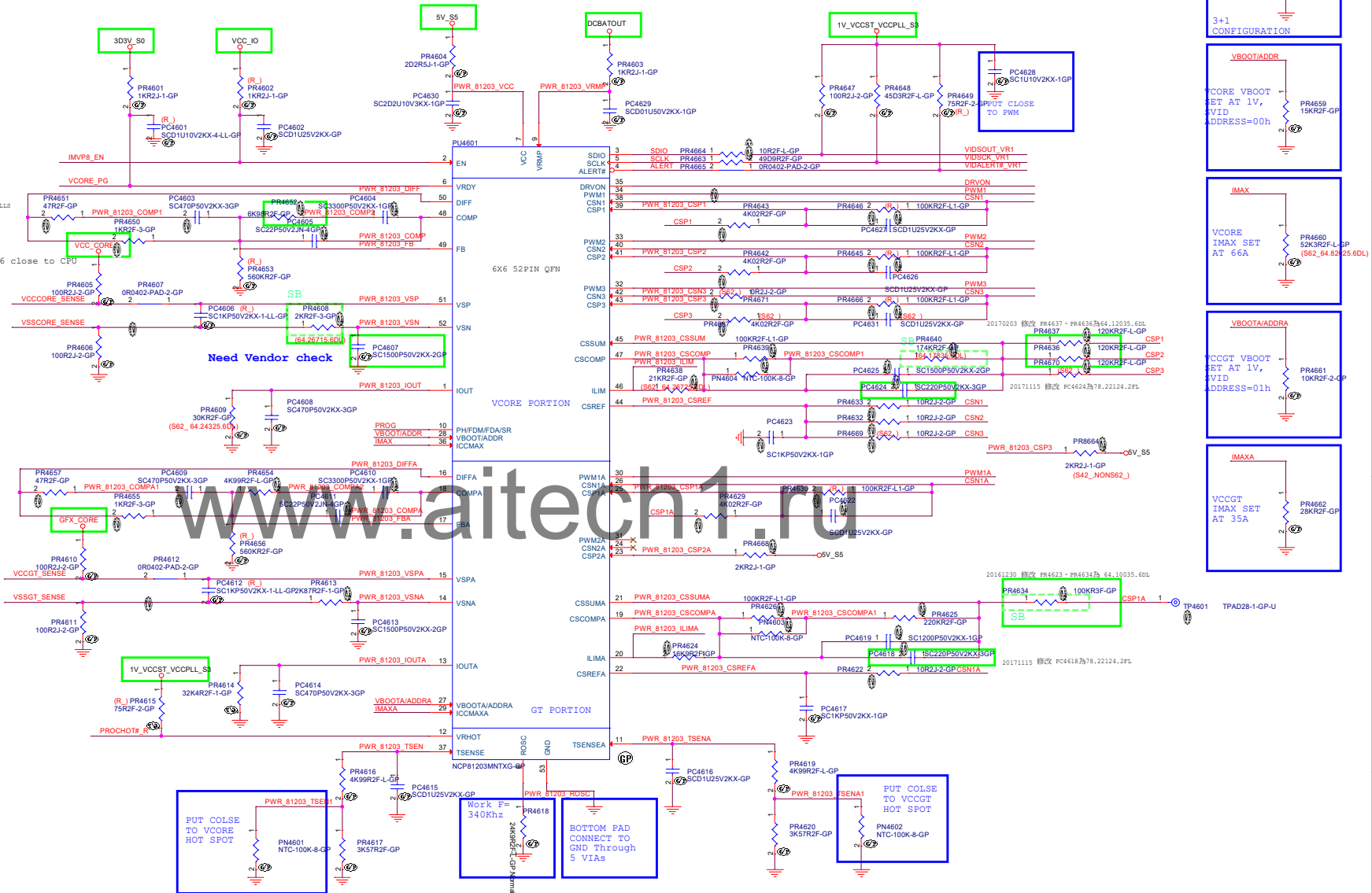
PWR_CORE/PWR_VCCGT

Intel Coffee Lake-S IMVP8 POWER 35W

- 24.40 IMVP8_EN >>
- 40 VCORE_PG <<
- 7 VCCORE_SENSE >>
- 7 VSSCORE_SENSE >>
- 7 VCCGT_SENSE >>
- 7 VSSGT_SENSE >>
- 6 PROCHOT#_R >>
- 6 VIDSOUT_VR1 >>
- 6 VIDSK_VR1 >>
- 6 VIDALERT#_VR1 >>
- 47.48 DRVON <<
- 47 PWM1 <<
- 47 CSN1 <<
- 47 PWM2 <<
- 47 CSN2 <<
- 47 PWM3 <<
- 47 CSN3 <<
- 47 PWM1A <<
- 48 CSN1A <<
- 47 CSP1 <<
- 47 CSP2 <<
- 47 CSP3 <<
- 48 CSP1A <<

20161230 修改 PR4652为64.69815.6DL15

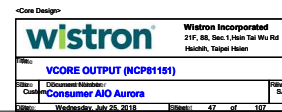
place PR4605, PR4606 close to CPU



20150312
Change U3601 PN 074.81203.0C73

084.36358.0037 AONS36358
Vgs @ 4.5V,
Id = 24A,
Rds(on) = 8.2mohm,

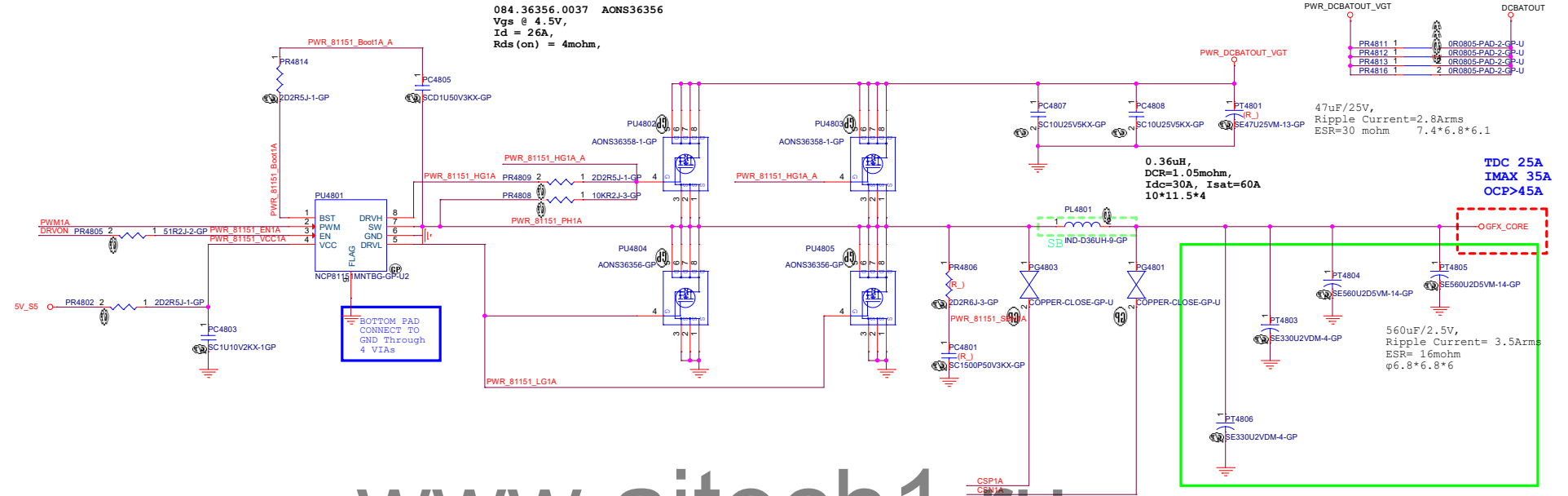
084.36356.0037 AONS36356
Vgs @ 4.5V,
Id = 26A,
Rds(on) = 4mohm,



PWR_VCCGT

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Vgs @ 4.5V,
Id = 24A,
Rds (on) = 8.2mohm,

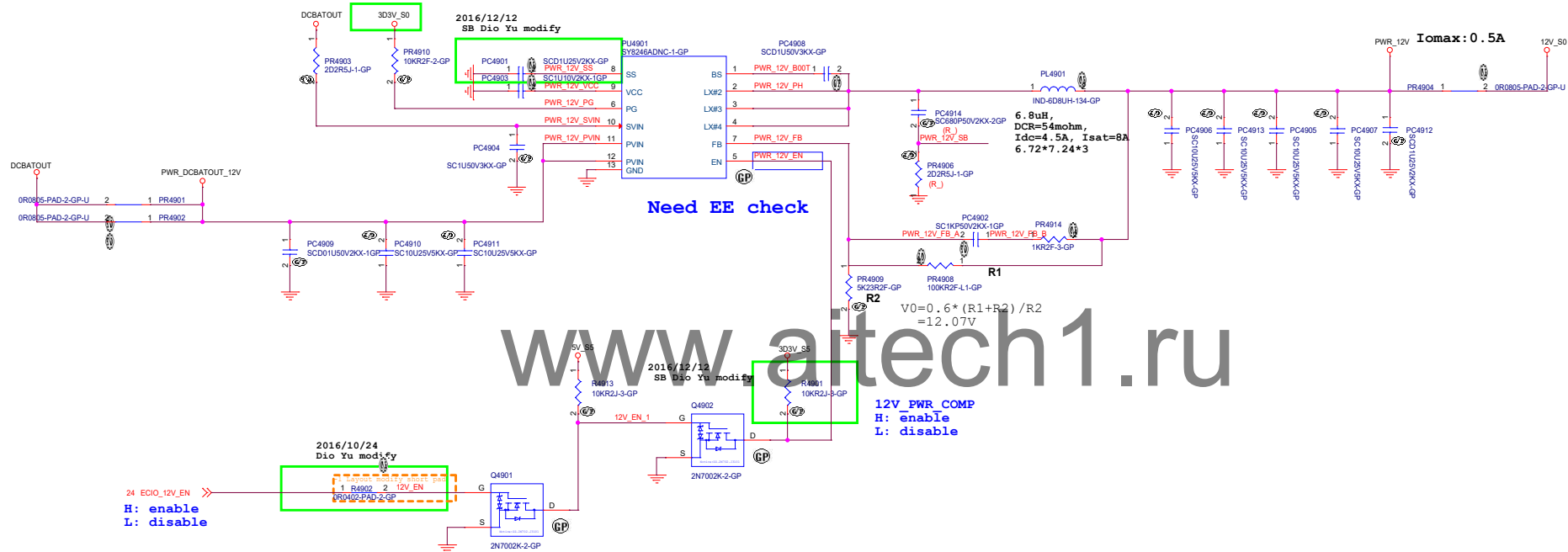
084.36356.0037 AONS36356
Vgs @ 4.5V,
Id = 26A,
Rds (on) = 4mohm,



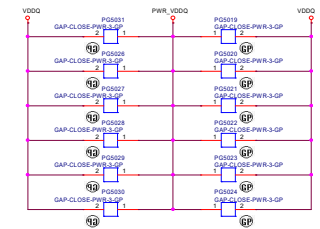
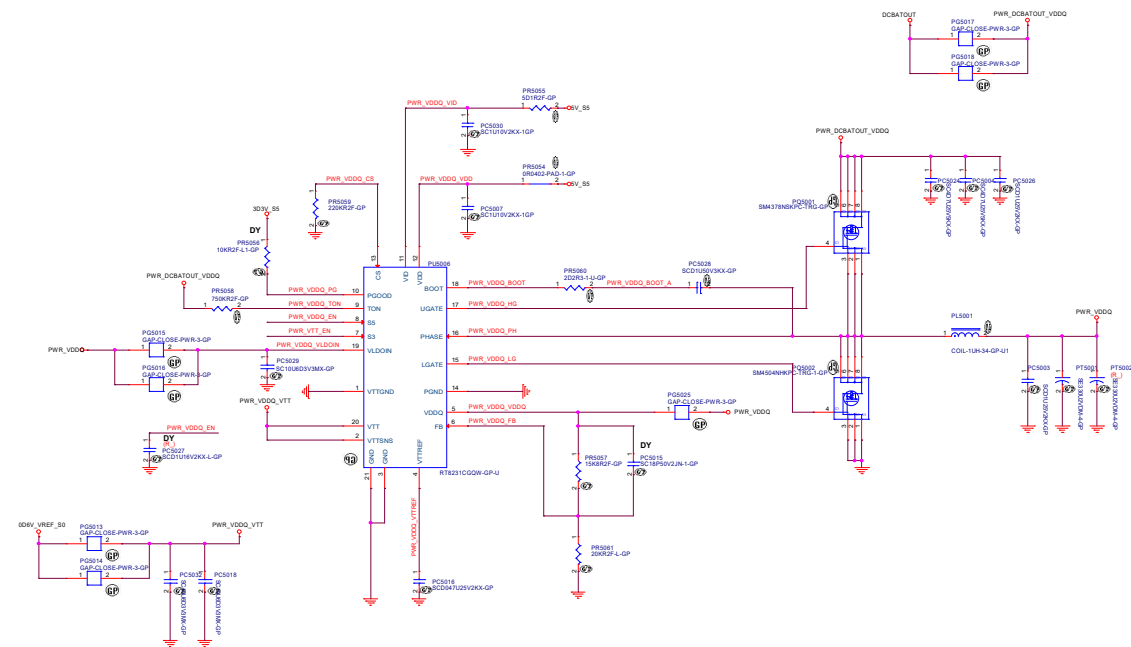
www.aitech1.ru

| | |
|--|--------------------------------|
| <Core Design> | |
| | |
| Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Hsinchu, Taipei Hsinchu | |
| Title: V_GT OUTPUT(NCP81151) | |
| Size: Customer | Rev: SA |
| Date: Wednesday, July 25, 2018 | Sheet: 48 of 107 |

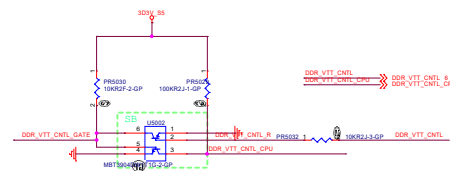
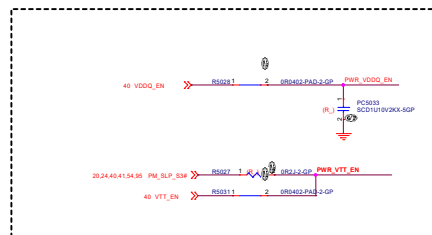
PWR_12V

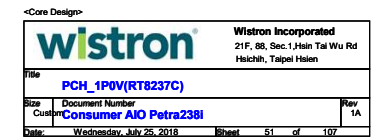


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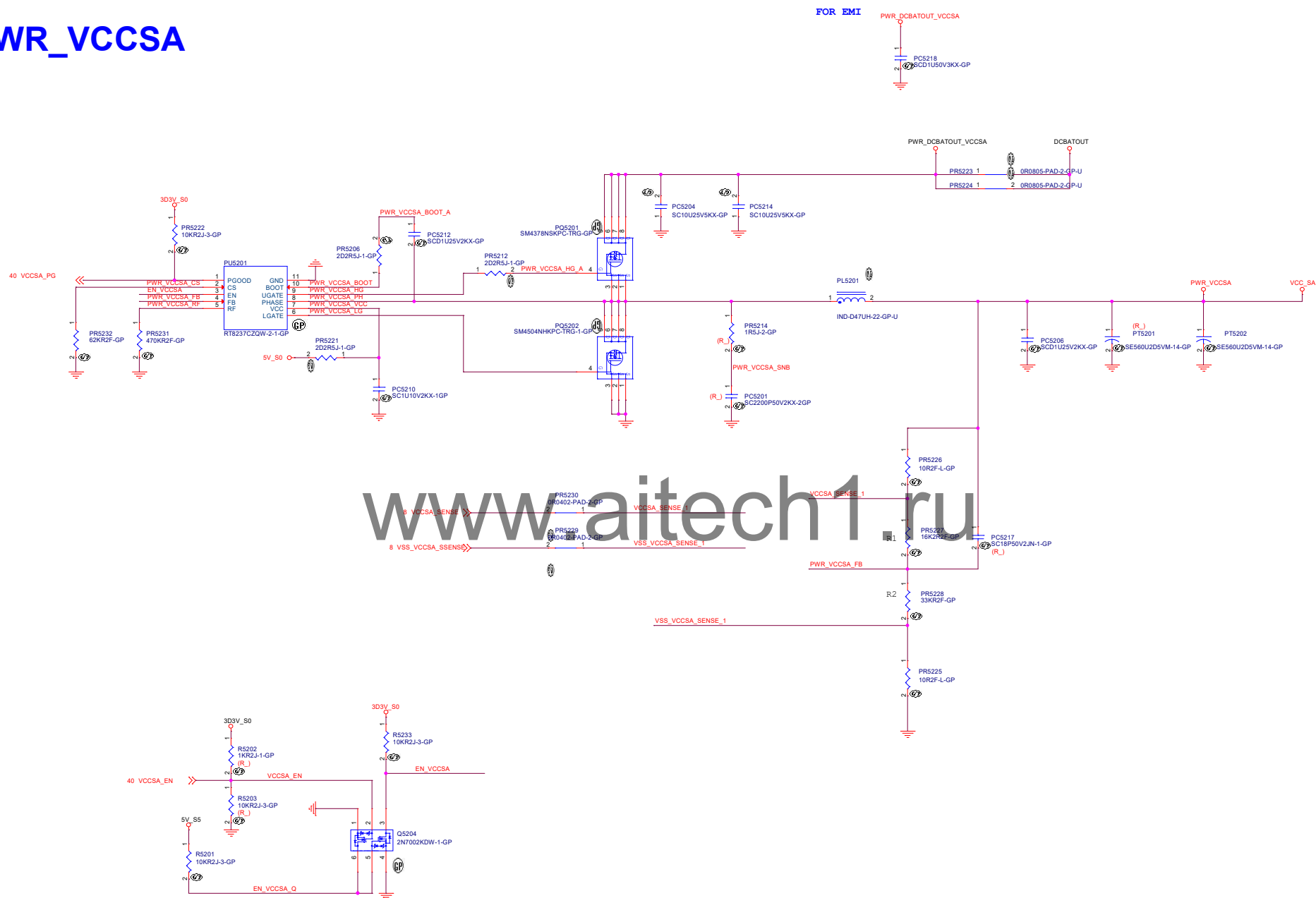


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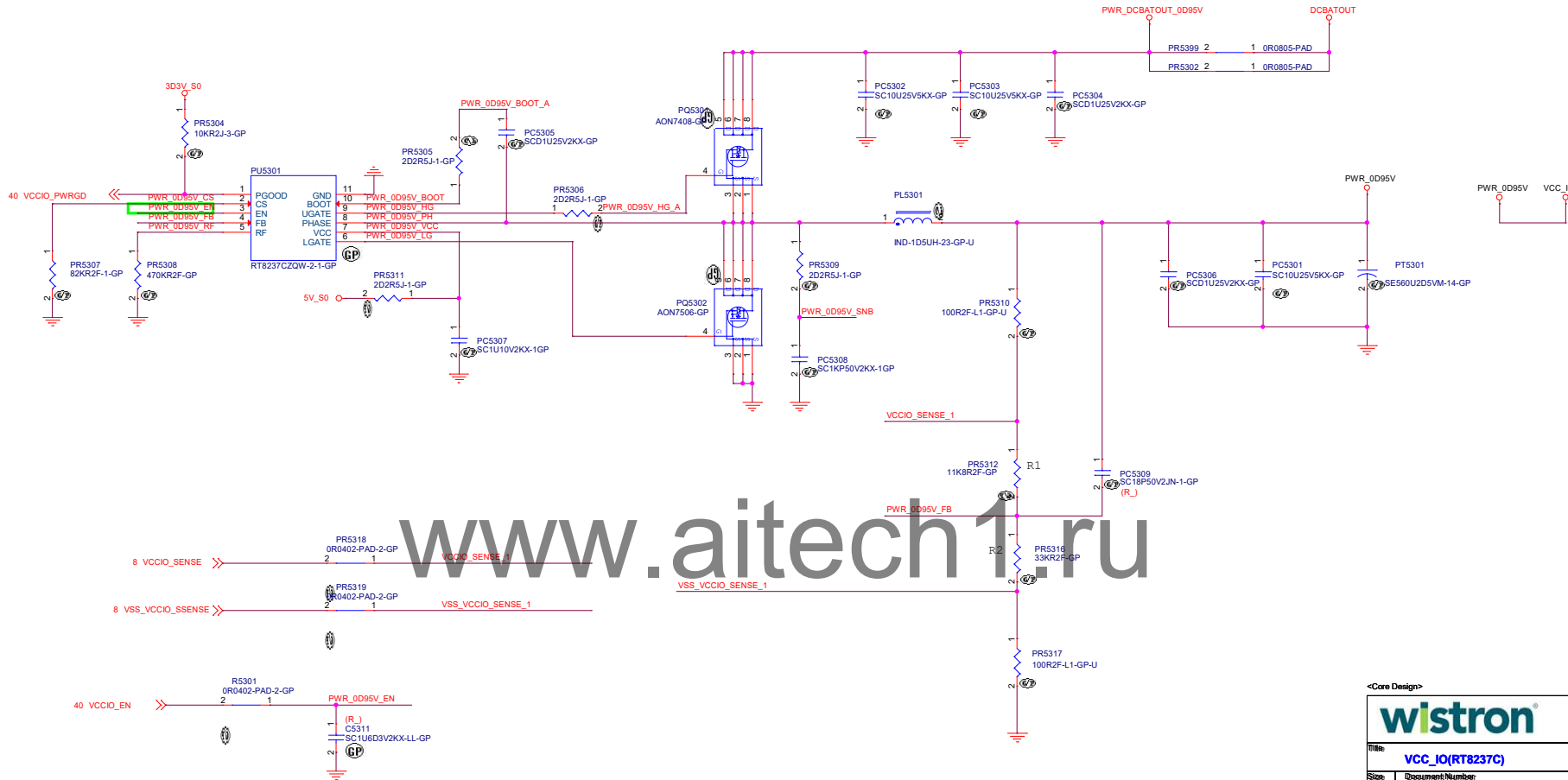




PWR_VCCSA

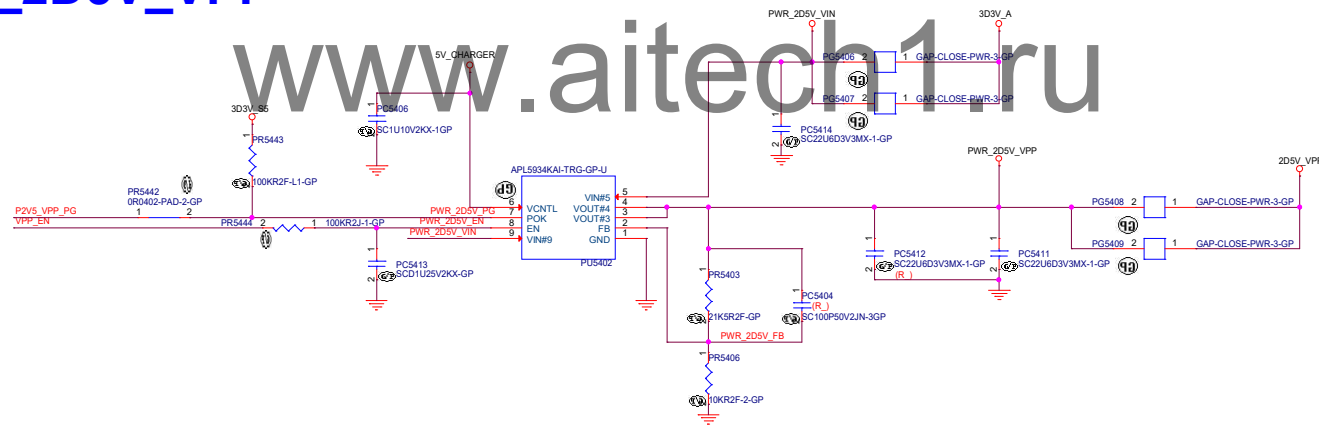


PWR_VCCIO



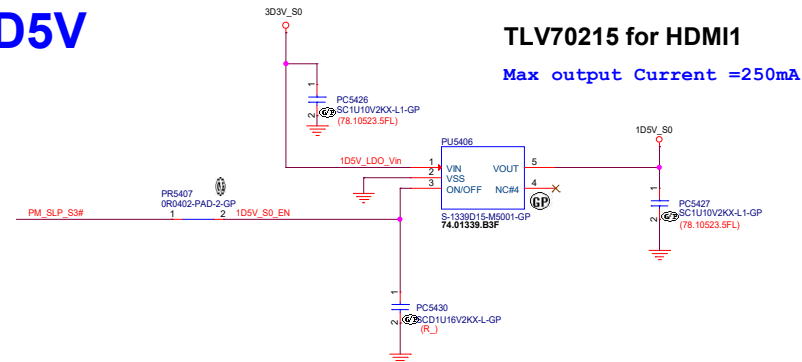
PWR_2D5V_VPP

40 P2V5_VPP_PG <<
40 VPP_EN >>



LDO: PWR_1D5V

20,24,40,41,50,95 PM_SLP_S3# >>



TLV70215 for HDMI1

Max output Current =250mA

<Core Design>

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Wistron Incorporated
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Haichih, Taipei Hsien

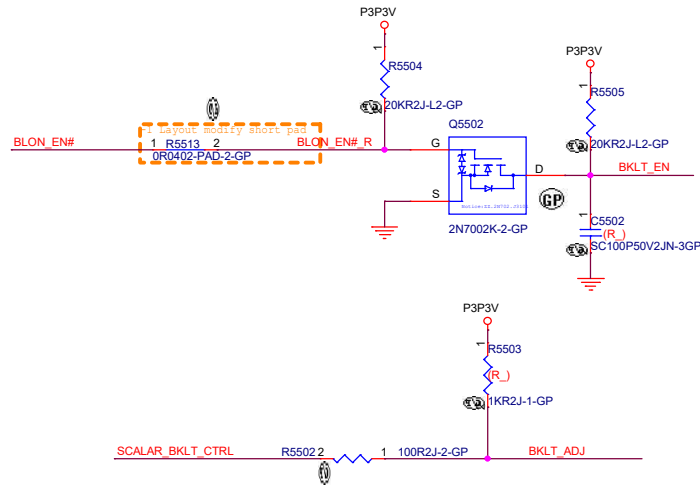
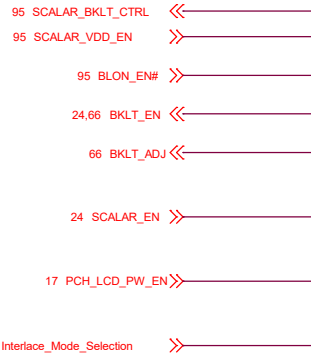
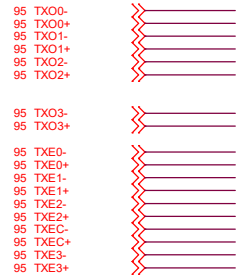
DCDC_2D5V (APL5930)

Customer: Consumer AIO Petra238i

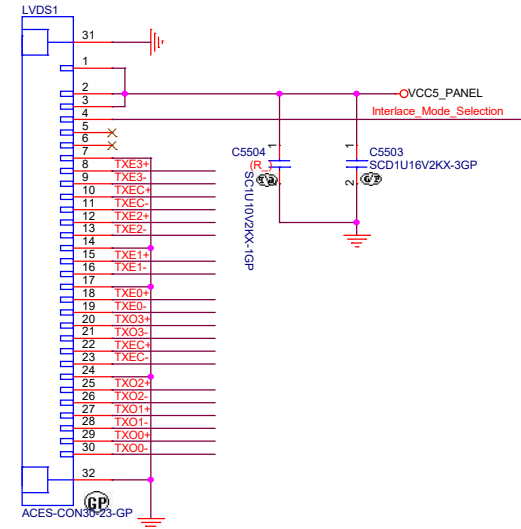
Date: Wednesday, July 25, 2018 Sheet: 54 of 107

SSID = VIDEO

LVDS

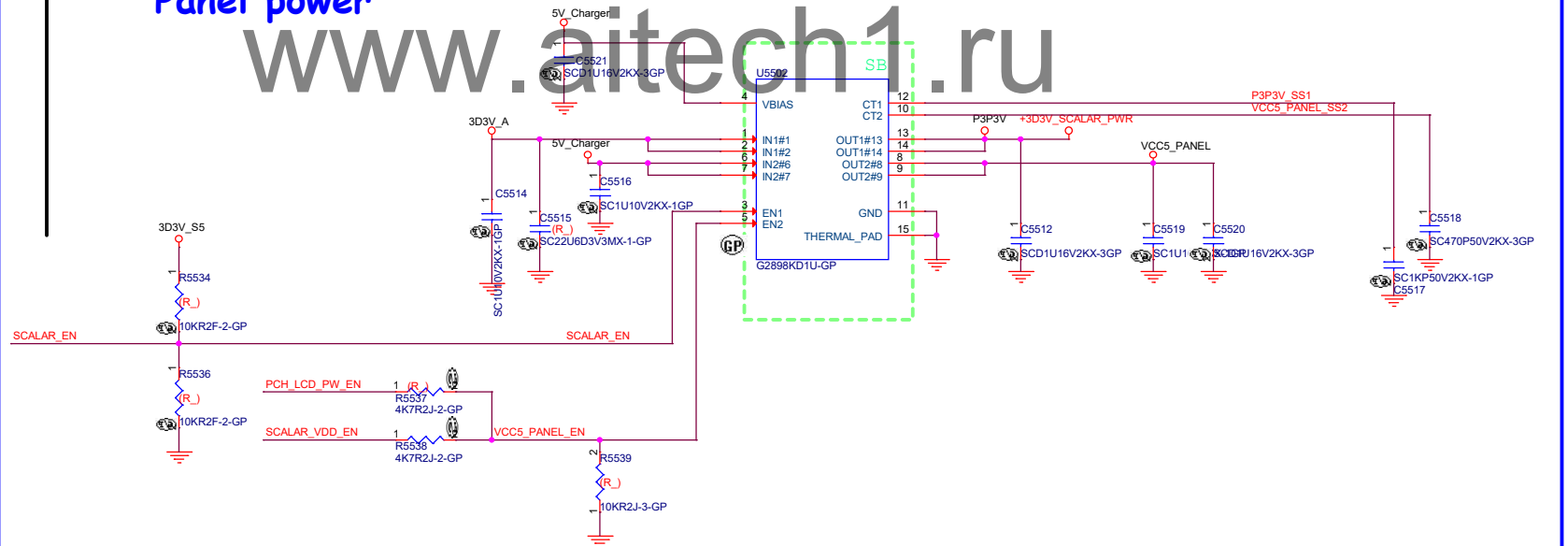


LVDS connector



Panel power

www.aitech1.ru



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd
Hsinchu, Taipei Hsien

Title:

LVDS Connector

Size:

Customer:

Consumer AIO Petra238i

Date:

Wednesday, July 25, 2018

Sheet:

55 of 107

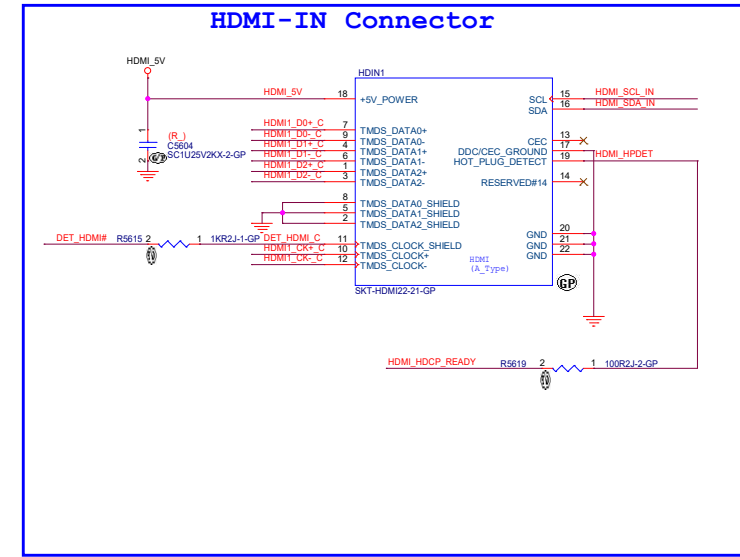
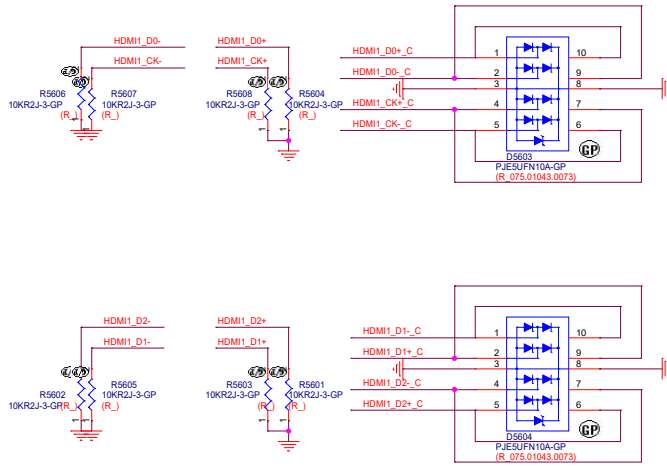
Rev:

1A

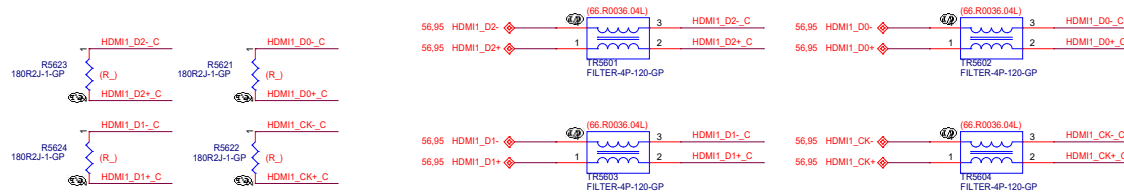
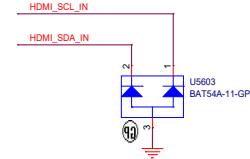
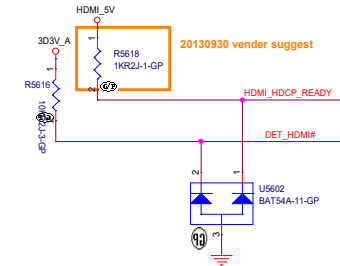
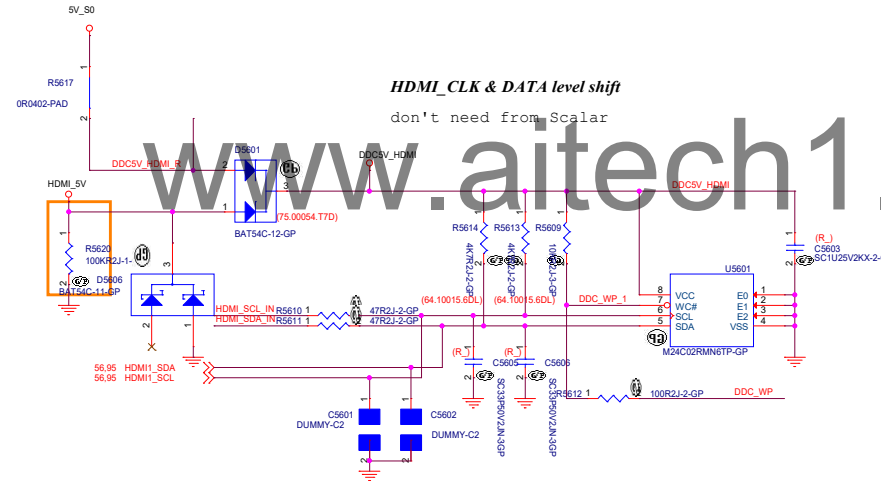
HDMI

56.95 HDMI1_D2+ <<<<<<
56.95 HDMI1_D2- <<<<<<
56.95 HDMI1_D1+ <<<<<<
56.95 HDMI1_D1- <<<<<<
56.95 HDMI1_D0+ <<<<<<
56.95 HDMI1_D0- <<<<<<
56.95 HDMI1_CK+ <<<<<<
56.95 HDMI1_CK- <<<<<<

24.56.95 DET_HDMI# <<<<<<
95 DDC_WP <<<<<<
56.95 HDMI1_SDA <<<<<<
56.95 HDMI1_SCL <<<<<<
95 HDMI_HDCP_READY <<<<<<
24.56.95 DET_HDMI# <<<<<<



HDMI_CLK & DATA level shift
don't need from Scalar



<Core Design>

wistron Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Haichih, Taipei Hsin

HDMI IN
Document Number: Consumer AIO Petra2381
Date: Wednesday, July 25, 2018 Sheet: 56 of 107

HDMI CONN



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<Core Design>

| | | | |
|---|--|---|-----------|
|  | | Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien | |
| Title DVI/CRT_(R) | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet | 58 of 107 |

Reserved

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<Core Design>

| | | | |
|---|--|---|-----------|
|  | | Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien | |
| Title Display switch_(R) | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet | 59 of 107 |

Reserved

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<Core Design>

| | | | |
|---|--------------------------|---|-----------|
|  | | Wistron Incorporated 21F, 88, Sec.1 Hsin Tai Wu Rd Haichih, Taipei Hsien | |
| Title | | HDD/ODD | |
| Size | Document Number | Rev | |
| Customer | Consumer AIO Aurora | SA | |
| Date | Wednesday, July 25, 2018 | Sheet | 60 of 107 |

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<Core Design>

| | | | |
|---|--|---|-----------|
|  | | Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien | |
| Title Mini PCIE Card TV Tuner | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet 61 of 107 | |

M.2 2230 / 1630 Key E Type

SMBUS

20 SMB_DATA_RESUME
20 SMB_CLK_RESUME

USB for BT

16 USB_PCH_PP14
16 USB_PCH_PN14

PCIE X1 & CLK

16 PCIE_RX_PCH_N7
16 PCIE_TX_WLAN_P7
16 PCIE_TX_WLAN_N7
18 PEG_CLK1_WLAN
18 PEG_CLK1_WLAN#
20 PCH_SUSCLK_WLAN

Control signal

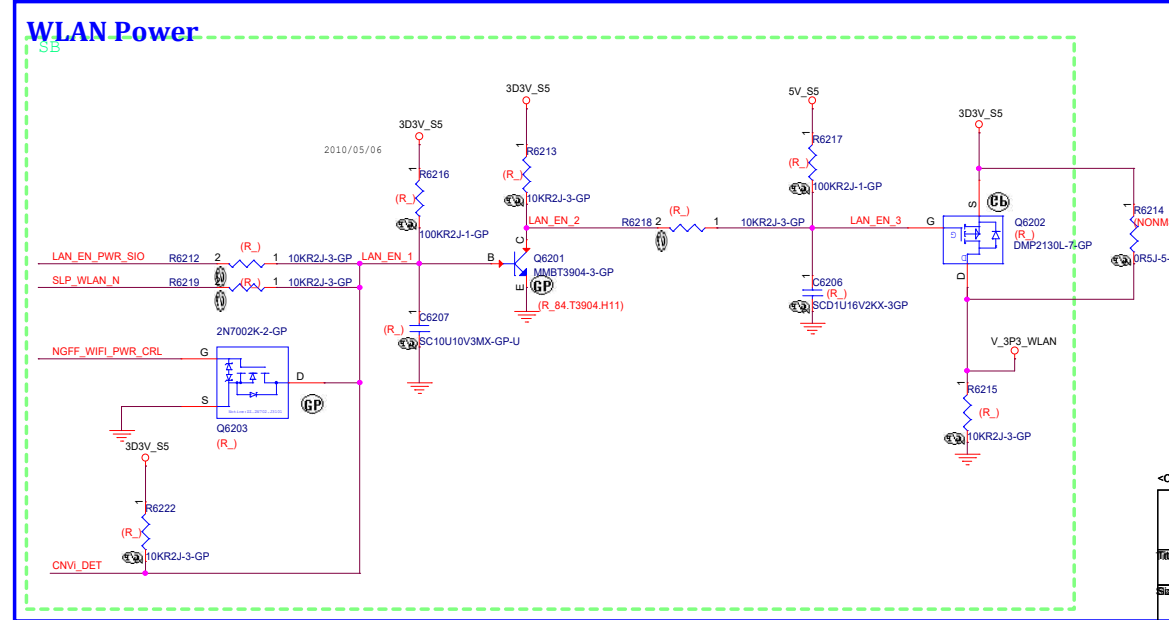
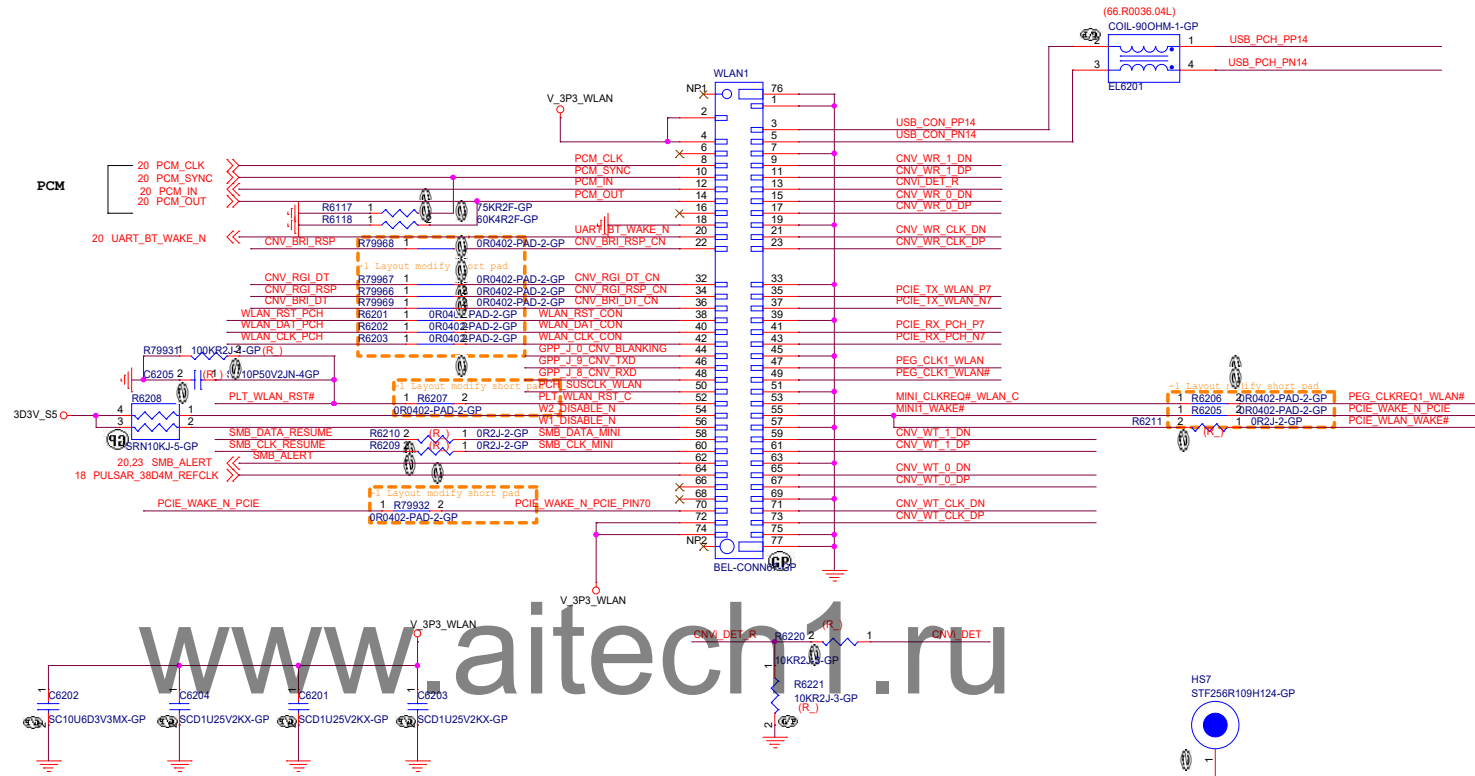
15 W1_DISABLE_N
15 W2_DISABLE_N
20 SLP_WLAN_N
24.62 LAN_EN_PWR_SIO
24 PCIE_WLAN_WAKER
24.62 LAN_EN_PWR_SIO
17 NGFF_WIFI_PWR_CRL

OTHERS

20 PCIE_WAKE_N_PCIE
24 PLT_WLAN_RST#
18 PEG_CLKREQ1_WLAN#

CNV1

17 CNV_WT_1_DN
17 CNV_WT_1_DP
17 CNV_WT_0_DN
17 CNV_WT_0_DP
17 CNV_WT_CLK_DN
17 CNV_WT_CLK_DP
17.23 CNV_BRI_RSP
17.23 CNV_RGI_DT
17.23 CNV_RGI_RSP
17.23 CNV_BRI_DT
17.23 CNV_BRI_DT
17.23 GPP_J_0 CNV_BLANKING
17.23 GPP_J_8 CNV_TXD
17 GPP_J_8 CNV_RXD
17 WLAN_RST_PCH
17 WLAN_DAT_PCH
17 WLAN_CLK_PCH
17 CNV_WR_1_DN
17 CNV_WR_1_DP
17 CNV_WR_0_DN
17 CNV_WR_0_DP
17 CNV_WR_CLK_DN
17 CNV_WR_CLK_DP
17 CNV_DET



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsinchu, Taipei Hsin

File: WLAN and BT-NGFF

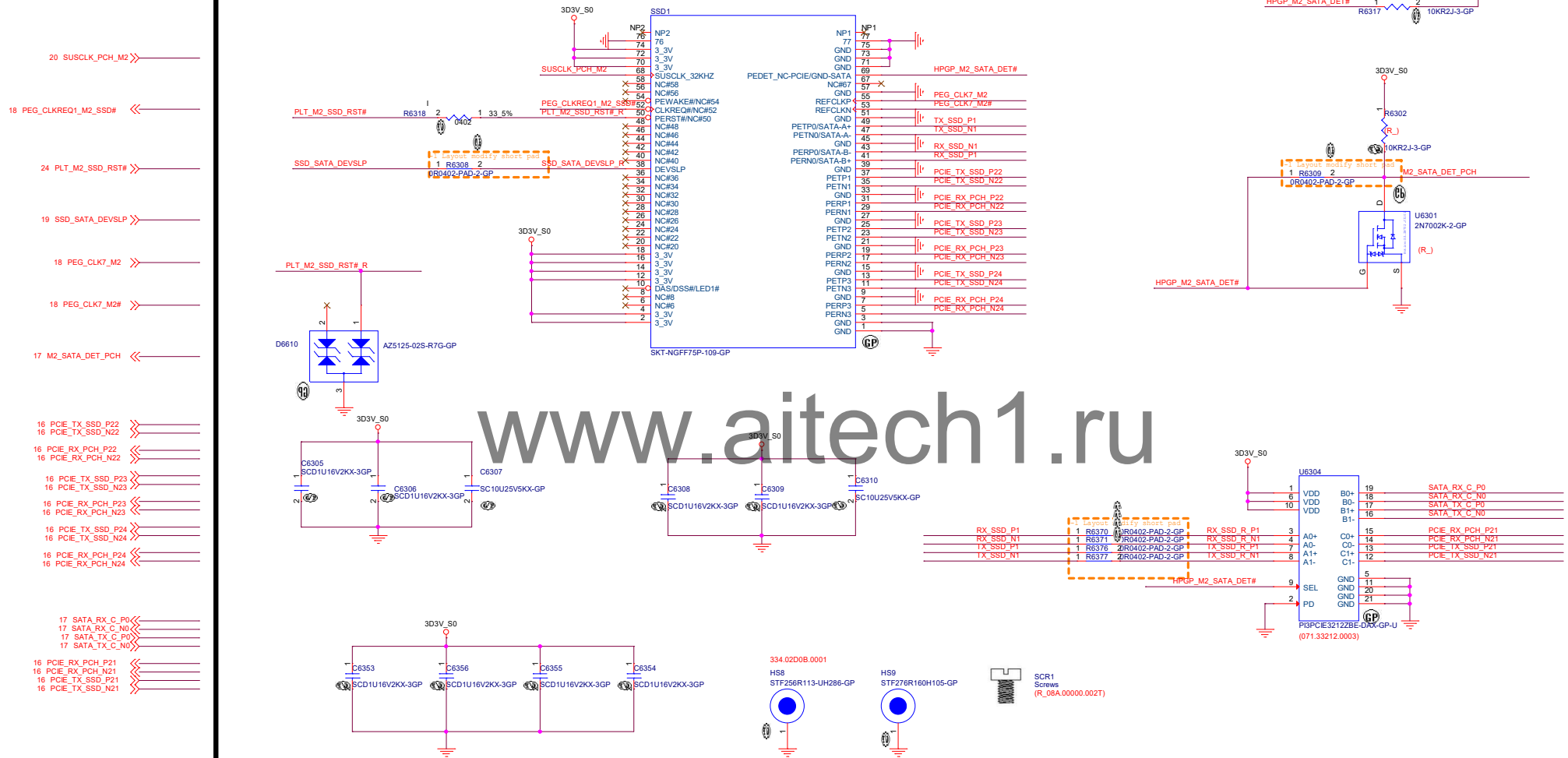
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Customer: Consumer AIO Petra2381

Date: Wednesday, July 25, 2018

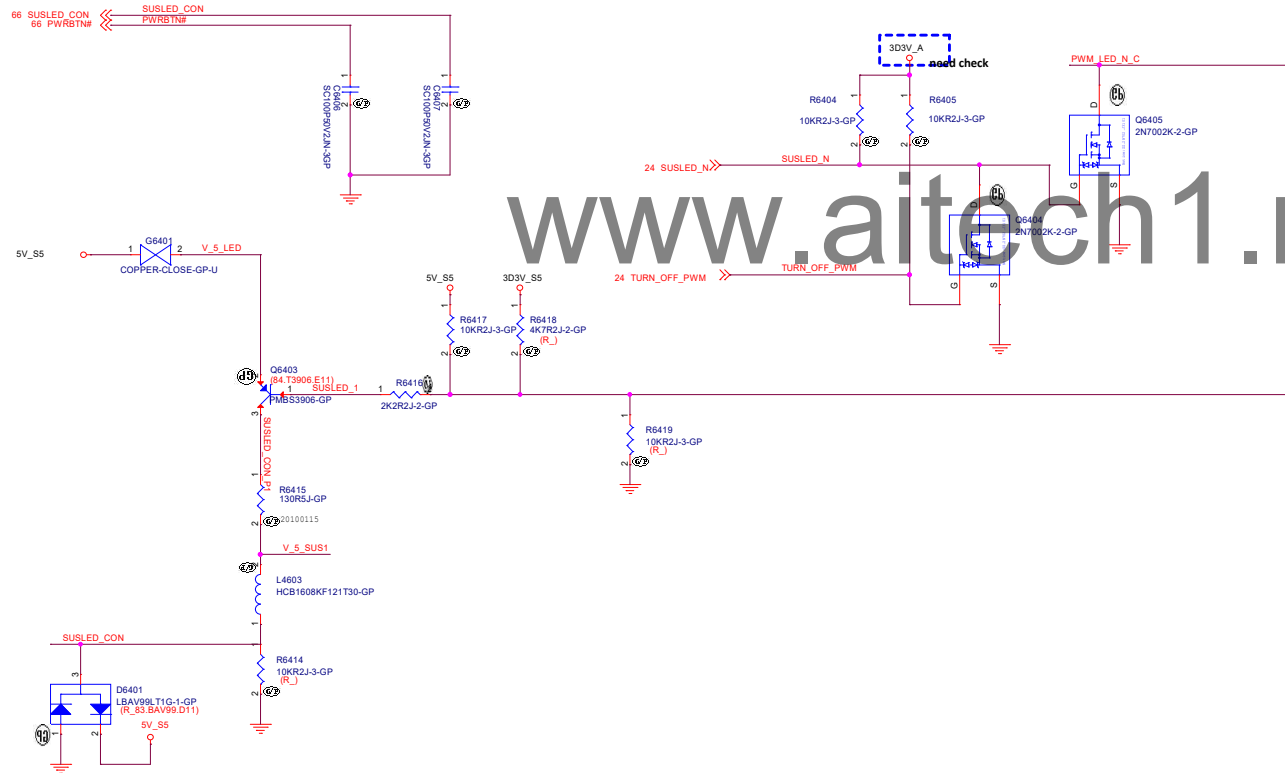
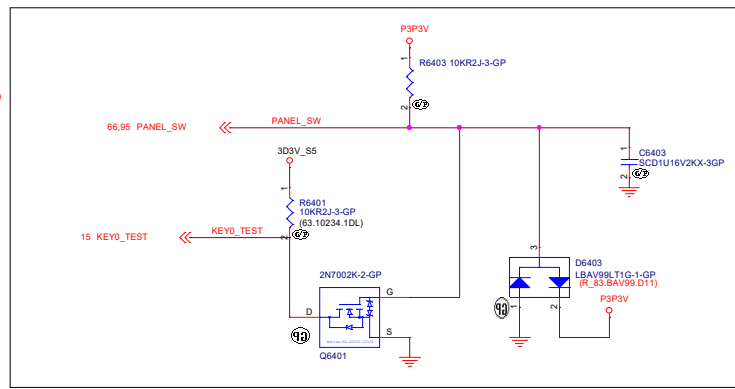
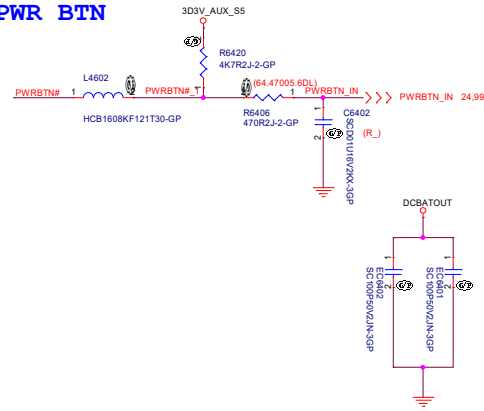
Sheet: 62 of 107

Rev 1A

M.2 Key M Type



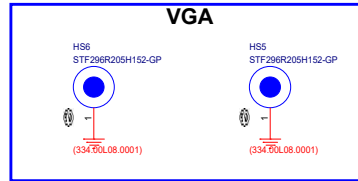
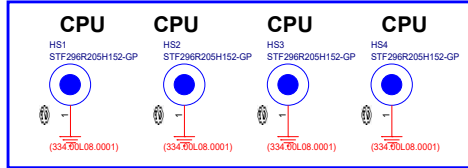
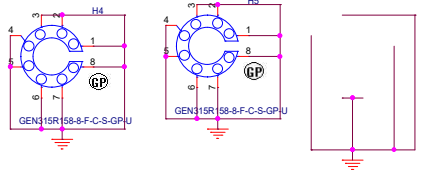
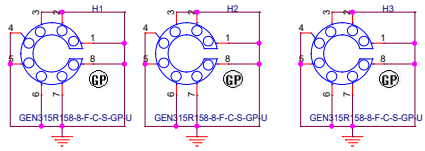
PWR BTN



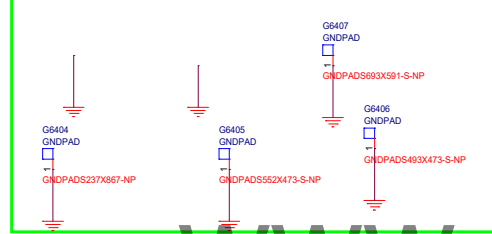
<Core Design>

| | | | |
|---|------------------------------------|---|-----------|
|  | | Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Hsinchu, Taipei Hsin | |
| File Title | PWR BT/Side Key/LED | | |
| Size Customer | Document Number Customer Number | | Rev |
| | Consumer AIO Petra238I | | |
| Date | Wednesday, July 25, 2018 | Sheet | 64 of 107 |

Stand off&Hole

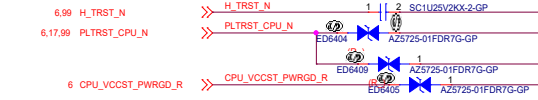


2016/11/28
Die-Vu modify

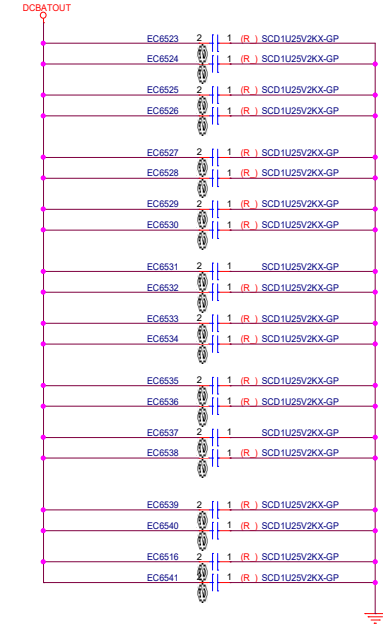
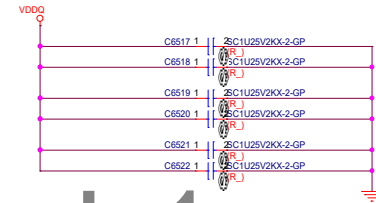
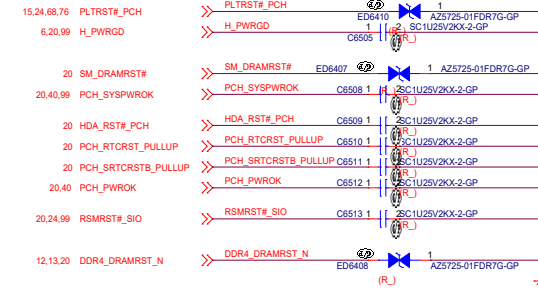


EMI CAP

EMI/ESD near CPU



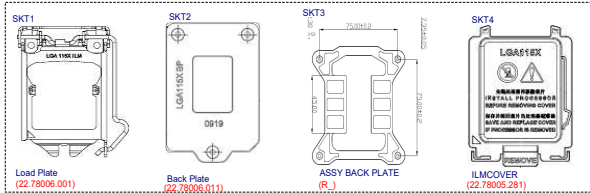
EMI/ESD near PCH



DUMMY BOM

Material part

SKYLAKE SOCKET



GSKT1
GASKET
(R_334.03508.0001)



GSKT2
GASKET
(R_334.0350F.0001)

GASKET FOR WIESON HDMI

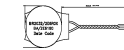
GASKET FOR TCONN HDMI

Battery Symbol



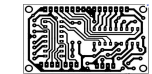
BAT3
BATTERY CR2032
(R_23.20068.001)

Vendor
P/N:
23.20068.001
23.20023.311
23.22063.001



BAT2
BATTERY BR2032_60MM
(R_23.24220.612)
Wire Length:60mm
耐高温>85C
Vendor
P/N:
23.21208.061
23.24220.612

PCB Symbol



PCB1
PCB
(R_)

HeatSink Symbol



PCB1
PCB
(R_)

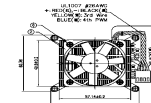
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P/N:
60.3MN01.011(second source)
60.3MN01.001

LABEL



Vendor
P/N:
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40.3KP03.011 -> 35 x 15mm
45.41107.021 -> 70 x 8mm
CARD
45.ACA01.0C1 -> 32 x 7mm
MIC CARD
345.02801.0001 -> 12 x 6mm

HeatSink+FAN Symbol

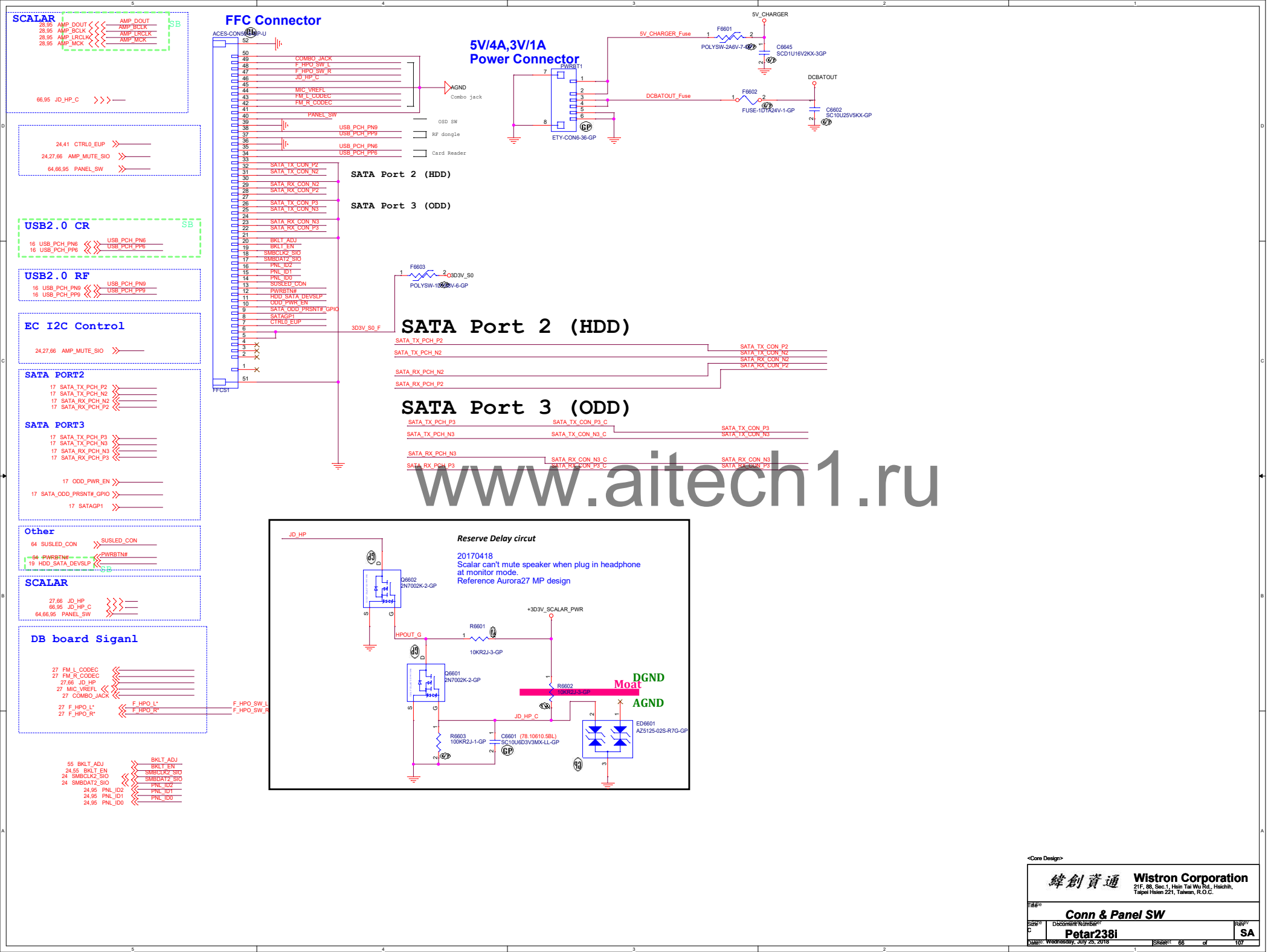


Vendor
P/N:

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Hsinchu, Taipei, Taiwan

| File | Stand off&EMI Cap&DUMMY BOM |
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| Sheet | Consumer AIO Petra2381 |
| Date | Wednesday, July 25, 2018 |
| Sheet | 65 of 107 |



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Document Number

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Date: Wednesday, July 25, 2018

Sheet

66

of

107

Rev

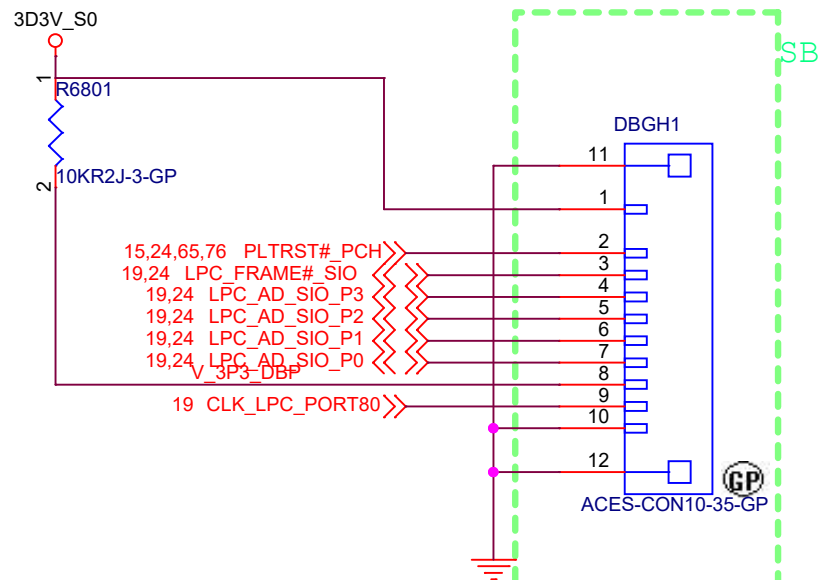
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| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet | 67 of 107 |



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Size
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Document Number
Consumer AIO Petra238i

Rev
1A

Date: Wednesday, July 25, 2018

Sheet 68 of 107

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| Date: | Wednesday, July 25, 2018 | Sheet 69 of 107 | |

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| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet | 70 of 107 |

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| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet 71 of 107 | |

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| Date: | Wednesday, July 25, 2018 | Sheet | 72 of 107 |

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| Date: | Wednesday, July 25, 2018 | Sheet 73 of 107 | |

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| Date: | Wednesday, July 25, 2018 | Sheet | 74 of 107 |

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| Date: | Wednesday, July 25, 2018 | Sheet | 75 of 107 |

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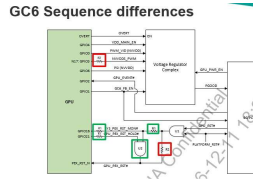
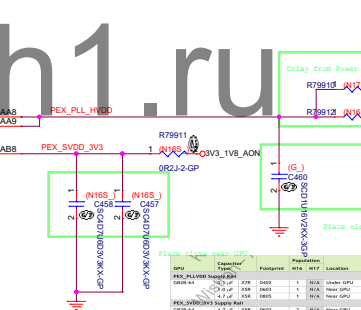
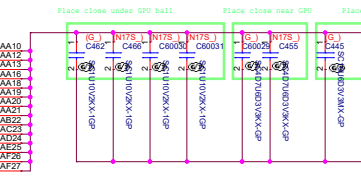
PCIE signal
3 PEG_RXP0
3 PEG_RXN0
3 PEG_C_TXP0
3 PEG_C_TXN0

3 PEG_RXP1
3 PEG_RXN1
3 PEG_C_TXP1
3 PEG_C_TXN1

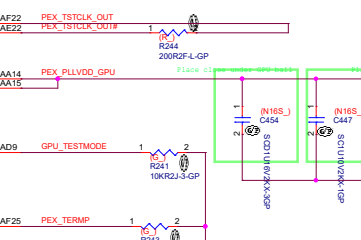
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3 PEG_RXN2
3 PEG_C_TXP2
3 PEG_C_TXN2

3 PEG_RXP3
3 PEG_RXN3
3 PEG_C_TXP3
3 PEG_C_TXN3

```

[illegible]

| Ball Location | N16/G82B-64 Ball Name | N17/G82C-64 Ball Name | What to do for an N17 or an N16/G82B-64 GPU |
|---------------|-----------------------|-----------------------|---|
| AA14 | PEX_PLLVDD | NC | Disconnect power supply |
| AA15 | PEX_PLLVDD | NC | Disconnect power supply |
| AB8 | PEX_SVDD_3V3 | NC | Disconnect power supply |



| | | |
|-----------------------|-----------------------|---|
| N17/GB28-64 Ball Name | N17/GB2C-64 Ball Name | What to do for an N17/GB2C-64 GPU on an N16/GB28-64 GPU board |
| STM0DE | NVJTAG_SEL | Leave pull-down resistor to GND |

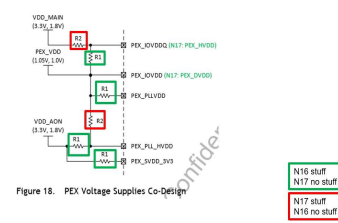
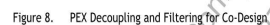
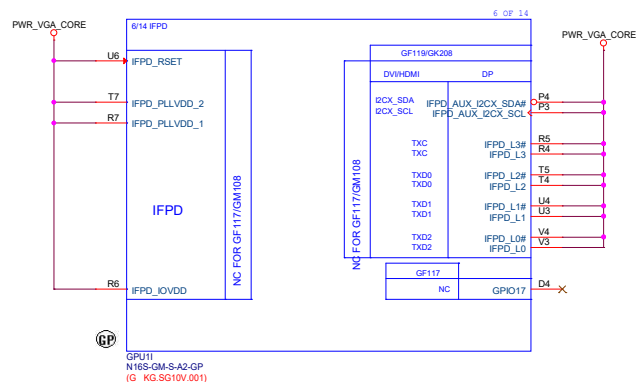
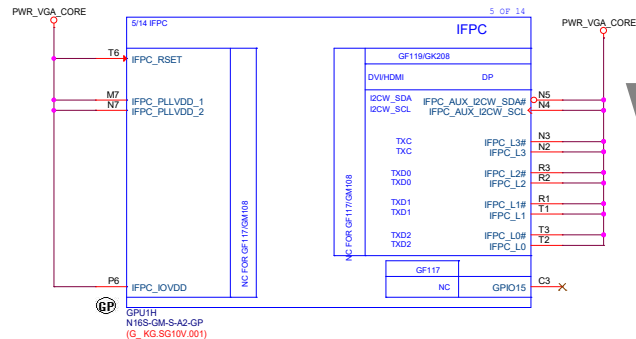
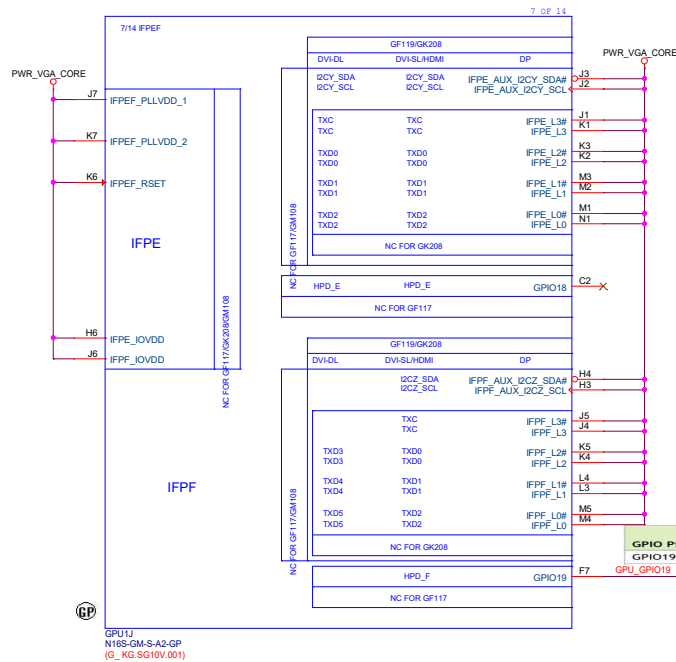
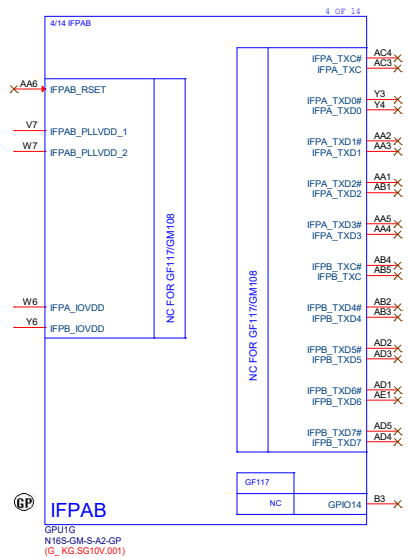


Figure 18. PEX Voltage Supplies Co-Design

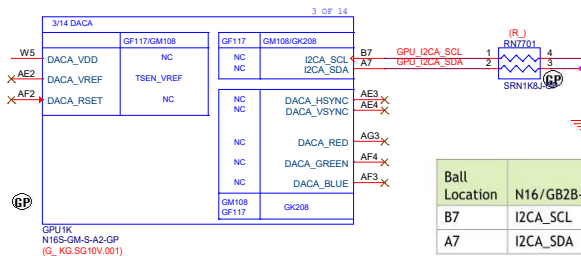
| GPU | Capacitor type | Population | | | |
|---|----------------|------------|-----|----------|------------------------------------|
| | | Footprint | N16 | Location | |
| N16_PEX_IDVDD1 [N16_PEX_IDVDD1 Supply Rail] | 1.0 μF | 355 | 0 | 1 | Under GPU |
| GE33-64 | 4.7 μF | 353 | 0 | 1 | Under GPU |
| GE32-64 | 10 μF | 353 | 0 | 2 | Near GPU |
| | 4.7 μF | N60 | 0 | 2 | Mixes between GPU and Power Supply |
| | 22 μF | 355 | 0 | 1 | Mixes between GPU and Power Supply |
| N16_PEX_IDVDD2 [N16_PEX_IDVDD2 Supply Rail] | 1.0 μF | 355 | 0 | 1 | Under GPU |
| GE33-64 | 4.7 μF | 353 | 0 | 1 | Under GPU |
| GE32-64 | 10 μF | 353 | 0 | 2 | Near GPU |
| | 4.7 μF | 0 | 0 | 2 | Mixes between GPU and Power Supply |
| | 22 μF | 355 | 0 | 1 | Mixes between GPU and Power Supply |

| GPU | Capacitor Type | Footprint | Population | | Location |
|--------------|-----------------|-----------|------------|-----|----------|
| PEX_FLL_HVDD | Supply Rail | | H16 | H17 | |
| GS2B-64s | 0.1 μ F X7R | 0402 | 1 | 1 | Near GPU |

| GPU | Capacitor Type | Footprint | Population | | |
|----------------------------------|----------------|-----------|------------|-----|--------------|
| | | | N16 | N17 | Location |
| PEX_PLLVD0 Supply Rail | | | | | |
| GR28-04 | 2.2 μ F | E7R D402 | 1 | N/A | Upper GPU |
| | 2.2 μ F | E3R 0603 | 1 | N/A | Neper GPU2 |
| | 4.7 μ F | E5R 0603 | 1 | N/A | Neper GPU3 |
| PEX_SVID0_V33 Supply Rail | | | | | |
| GR28-04 | 10 μ F | E3R 0603 | 9 | N/A | Alameda GPU1 |



| Ball Location | N16/GB2B-64 Ball Name | N17/GB2C-64 Ball Name | What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board |
|---------------|-----------------------|-----------------------|---|
| AE2 | NC | TS_VREF | Name change only |



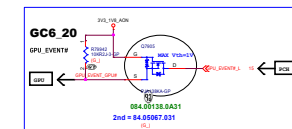
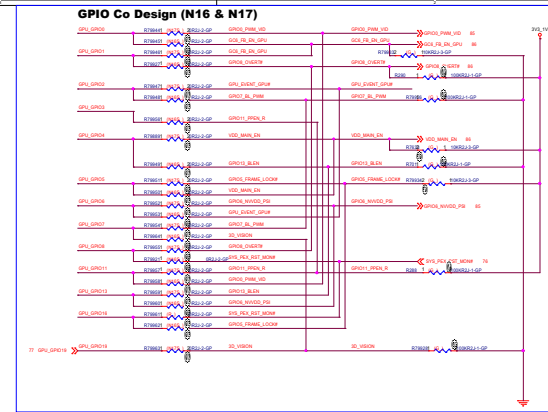
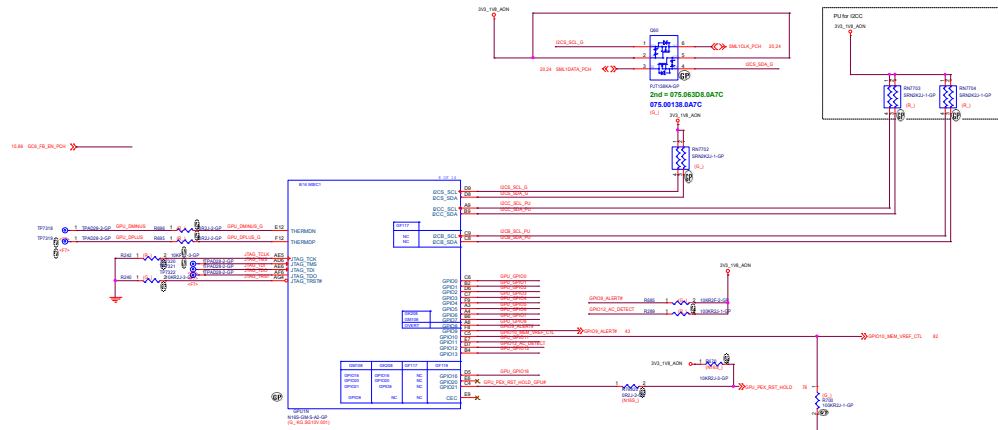
| GPIO Pin | N16 GPU Function | N16 GPU Function on Co-Design | N17 GPU Function | Comments |
|----------|----------------------|-------------------------------|------------------|----------|
| GPIO19 | HPD_IFPF or HPD_IFPB | 3D VISION | 3D VISION | |

GPU_GPIO19 → GPU_GPIO19 79

| Ball Location | N16/GB2B-64 Ball Name | N17/GB2C-64 Ball Name | What to do for an N17/GB2C-64 GPU on an N16/GB2B-64 GPU board |
|---------------|-----------------------|-----------------------|---|
| B7 | I2CA_SCL | GPIO23 | Leave unconnected |
| A7 | I2CA_SDA | GPIO22 | Leave unconnected |

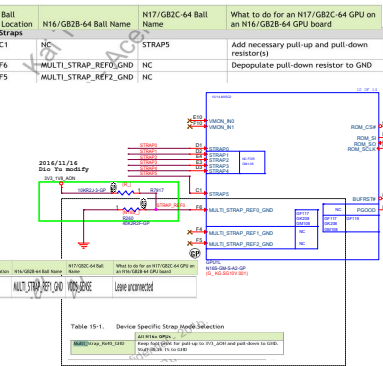
NOTE 4: DEV0_SEL default setting is 0

NOTE 5: PCIe_CFG default setting is 0 (high power/high swing). For some NB projects, this should be 1 (lower power/low swing)

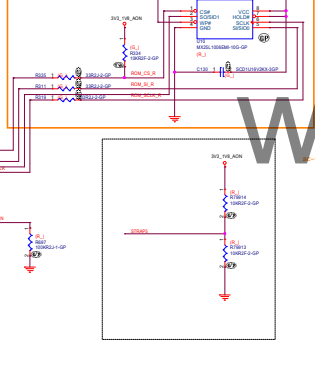


| GPIO Pin | N16 GPU Function | N16 GPU Function on Co-Design | N17 GPU Function | Comments |
|----------|----------------------|-------------------------------|--------------------|-----------------------------|
| GPIO0 | GC6_FB_EN | PWM_VID | PWM_VID | N17 PWM_VID for NVDD supply |
| GPIO1 | MEM_VDD_CTL | GC6_FB_EN | GC6_FB_EN | |
| GPIO2 | LCD_BL_PWM | GPU_EVENT# | GPU_EVENT# | |
| GPIO3 | LCD_VCC | RESERVED | RESERVED | |
| GPIO4 | LCD_BLEN | 3V3_MAIN_EN | 1V8_MAIN_EN | |
| GPIO5 | 3V3_MAIN_EN | FRAME_LOCK# | FRAME_LOCK# | |
| GPIO6 | GPU_EVENT# | PSI | PSI | N17 PSI for NVDD supply |
| GPIO7 | 3D VISION | LCD_BL_PWM | LCD_BL_PWM | |
| GPIO8 | SYS_PEX_RST_MON# | IFPE_HPD | IFPE_HPD | |
| GPIO9 | THERM_ALERT | THERM_ALERT | THERM_ALERT | Same |
| GPIO10 | MEM_VREF_CTL | MEM_VREF_CTL | MEM_VREF_CTL | Same |
| GPIO11 | PWM_VID | LCD_VDD | LCD_VDD | |
| GPIO12 | PWR_LEVEL | PWR_LEVEL | PWR_LEVEL | Same |
| GPIO13 | PSI | LCD_BLEN | LCD_BLEN | |
| GPIO14 | HPD_IFPA | HPD_IFPA | HPD_IFPA | Same |
| GPIO15 | HPD_IFPB | HPD_IFPB | HPD_IFPB | Same |
| GPIO16 | FRAME_LOCK# | SYS_PEX_RST_MON# | RESERVED | |
| GPIO17 | HPD_IFPD | HPD_IFPD | HPD_IFPD | Same |
| GPIO18 | HPD_IFPE | HPD_IFPE | HPD_IFPE | Same |
| GPIO19 | HPD_IFPE or HPD_IFPB | 3D VISION | 3D VISION | |
| GPIO20 | RESERVED | IFPE_HPD | RESERVED | |
| GPIO21 | GPU_PEX_RST_HOLD# | GPU_PEX_RST_HOLD# | RESERVED (OC_WARN) | |
| GPIO22 | RESERVED | | New N17 GPIO | |
| GPIO23 | RESERVED | | New N17 GPIO | |

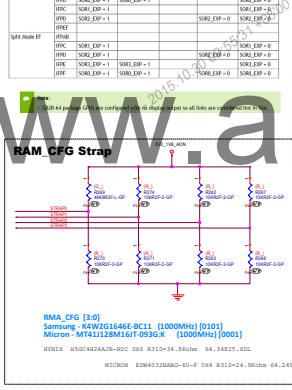
STRAP



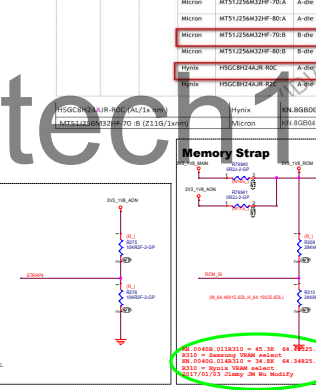
External BIOS ROM



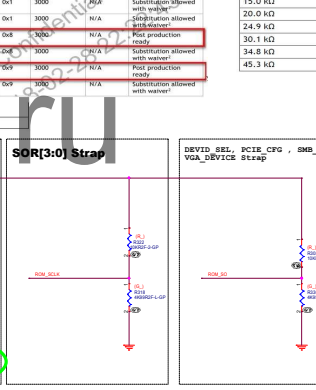
RAM CFG Strap



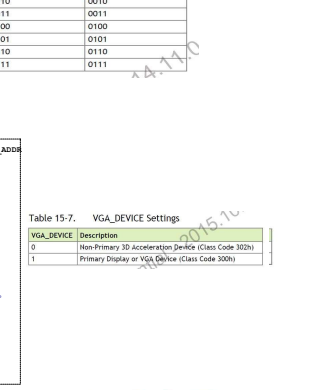
Memory Strap



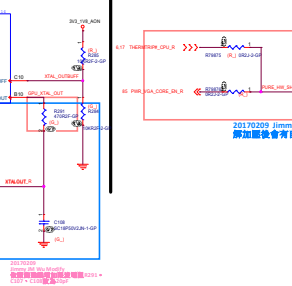
SOR[3:0] Strap



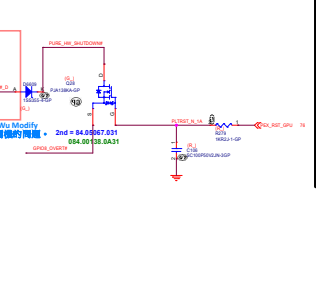
DEVID_SEL, PCIe_CFG, SMB_ATT_ADDR



RMA_CFG [3:0]



XTAL



THERMAL PROTECTION

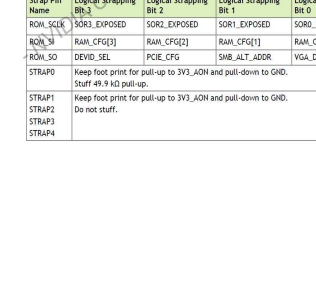


Table 15-1: Device Specific Strap Table

| Strap Name | Strap Value | Strap Description |
|--------------------|-------------|-------------------|
| DEV0_SEL | 0 | Default setting |
| PCIe_CFG | 0 | Default setting |
| SMB_ATT_ADDR | 0 | Default setting |
| DEVID_SEL | 0 | Default setting |
| RMA_CFG[3:0] | 0000 | Default setting |
| XTAL | 0 | Default setting |
| THERMAL_PROTECTION | 0 | Default setting |

Table 13. N16V-GMR1 and N16S-LG-/GMR-/GTR GDDR5 Recommended Memories

| Memory Type | FBVDDQ | Memory Density | Vendor | Manufacturer Part Number | Die Revision | Strap | Memory Speed Grade (MHz) | Memory Power Consumption | Status |
|-------------|--------|----------------|--------|--------------------------|--------------|-------|--------------------------|--------------------------|---------------------------------|
| Memory | 1.8V | 3000 | Micron | MT51256A0320F-40-A | A-die | 0x1 | 3000 | N/A | Substitution allowed with wafer |
| | | | | MT51256A0320F-70-A | A-die | 0x1 | 3000 | N/A | Substitution allowed with wafer |
| | | | | MT51256A0320F-80-A | B-die | 0x1 | 3000 | N/A | Substitution allowed with wafer |
| | | | | MT51256A0320F-80-B | B-die | 0x1 | 3000 | N/A | Substitution allowed with wafer |
| Memory | 1.8V | 3000 | Hynix | H5G82408R-B0C | A-die | 0x1 | 3000 | N/A | Substitution allowed with wafer |
| | | | | H5G82408R-B0C | A-die | 0x1 | 3000 | N/A | Substitution allowed with wafer |

Table 15-2. Resistance Mapping to Hex Values

| Resistor Values | Pull-Up to 3V3_MAIN | Pull-Down to GND |
|-----------------|---------------------|------------------|
| 4.99 kΩ | 1000 | 0000 |
| 10.0 kΩ | 1001 | 0001 |
| 15.0 kΩ | 1010 | 0010 |
| 20.0 kΩ | 1011 | 0011 |
| 24.9 kΩ | 1100 | 0100 |
| 30.1 kΩ | 1101 | 0101 |
| 34.8 kΩ | 1110 | 0110 |
| 45.3 kΩ | 1111 | 0111 |

Table 15-7. VGA_DEVICE Settings

| VGA_DEVICE | Description |
|------------|---|
| 0 | Non-Primary 3D Accelerator (Device Class Code 3020) |
| 1 | Primary Display or VGA Device (Class Code 3000) |

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-Level Mode Strapping

| Strap Pin Name | Logical Strapping Bit 3 | Logical Strapping Bit 2 | Logical Strapping Bit 1 | Logical Strapping Bit 0 |
|----------------|---|-------------------------|-------------------------|-------------------------|
| RAM_CLK | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| RAM_CS | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0] |
| DEV0_SEL | PCI_CFG | PCI_CFG | SMB_ATT_ADDR | VGA_DEVICE |
| STRAP0 | Keep foot print for pull-up to 3V3_AON and pull-down to GND. Sturt 49.9 kΩ pull-up. | | | |
| STRAP1 | Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not sturt. | | | |
| STRAP2 | | | | |
| STRAP3 | | | | |
| STRAP4 | | | | |

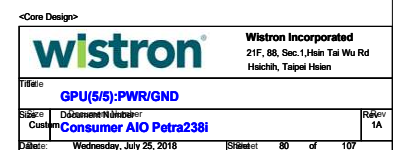
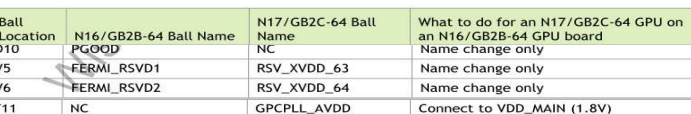
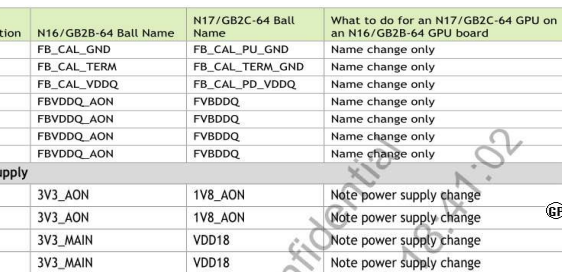
TABLE 1: STRAP DECODE ACCORDING TO TERMINATION RESISTANCE/VOLTAGE

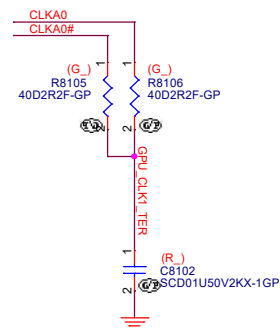
| TERMINATION RESISTANCE | 3V3 VOLTAGE | GND |
|------------------------|-------------|------|
| 5K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 25K | 1100 | 0100 |
| 30K | 1101 | 0101 |
| 35K | 1110 | 0110 |
| 45K | 1111 | 0111 |

12 OF 14

| Pin Label | Signal |
|-----------|-----------|
| B26 | FBVDDQ_01 |
| C25 | FBVDDQ_02 |
| E23 | FBVDDQ_03 |
| E26 | FBVDDQ_04 |
| F14 | FBVDDQ_05 |
| F21 | FBVDDQ_06 |
| G13 | FBVDDQ_07 |
| G14 | FBVDDQ_08 |
| G15 | FBVDDQ_09 |
| G16 | FBVDDQ_10 |
| G18 | FBVDDQ_11 |
| G19 | FBVDDQ_12 |
| G20 | FBVDDQ_13 |
| G21 | FBVDDQ_14 |
| L22 | FBVDDQ_19 |
| L24 | FBVDDQ_20 |
| L26 | FBVDDQ_21 |
| M21 | FBVDDQ_22 |
| N21 | FBVDDQ_23 |
| R21 | FBVDDQ_24 |
| T21 | FBVDDQ_25 |
| V21 | FBVDDQ_26 |
| W21 | FBVDDQ_27 |

GF117
 GF119
 GK208






| | | | |
|----------------|---------------------------|-----------------------------|----------------------------|
| | HYNIX 4GBITS (128Mx32) | SAMSUNG 4GBITS (128Mx32) | Micron 4GBITS (128Mx32) |
| VRAM1 VRAM2 | H5GC4H24AJR-T2C | K4G41325FC-HC03 | EDW4032BABG-60-F-D |



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| Date: | Wednesday, July 25, 2018 | Sheet 83 of 107 | |

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Title

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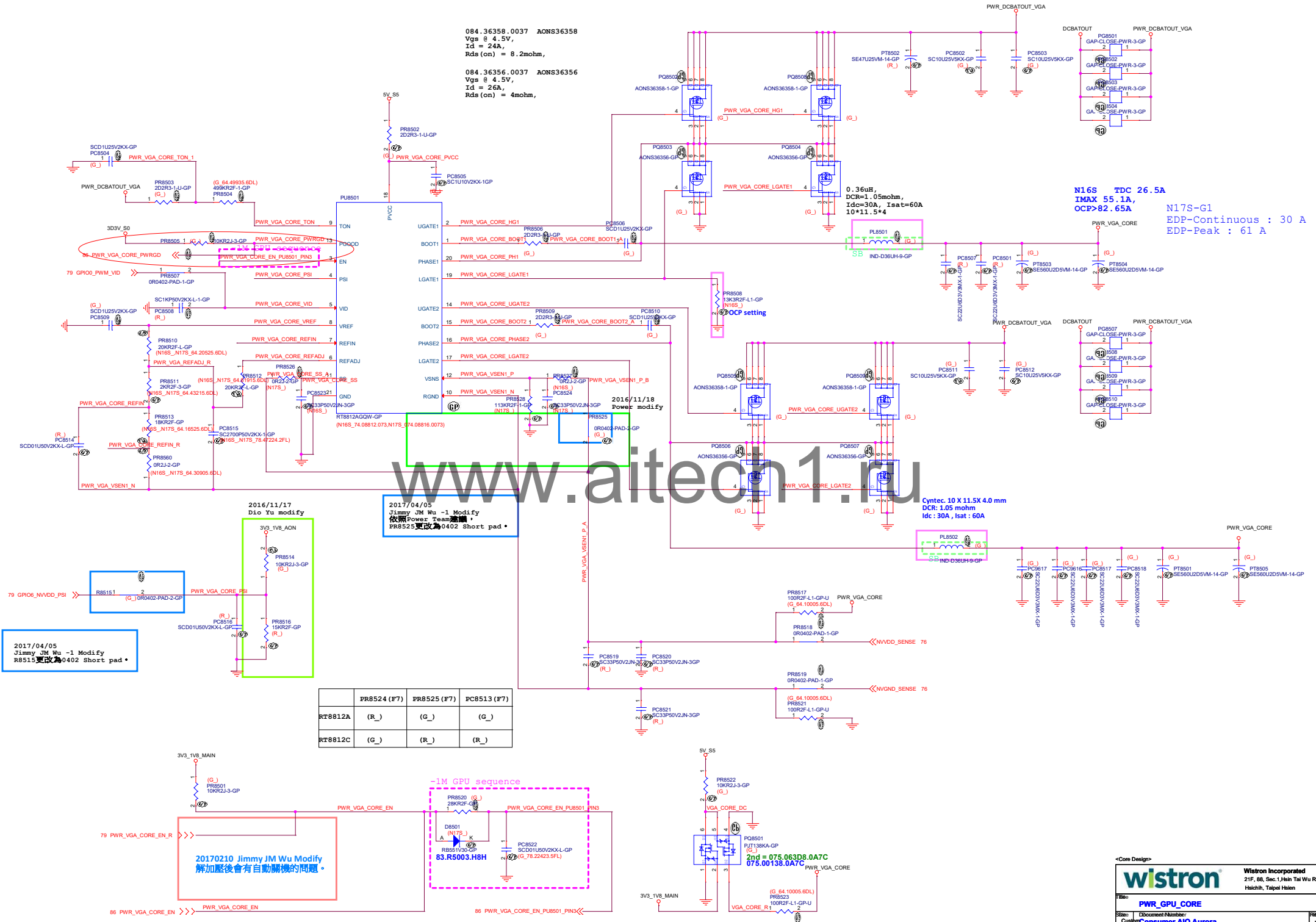
Rev
1A

Date: Wednesday, July 25, 2018

Sheet 84 of 107

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084.36356.0037 AONS36356
Vgs @ 4.5V,
Id = 26A,
Rds(on) = 4mohm,



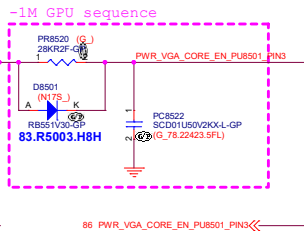
2017/04/05
Jimmy JM Wu -1 Modify
R8515更改为0402 Short pad *

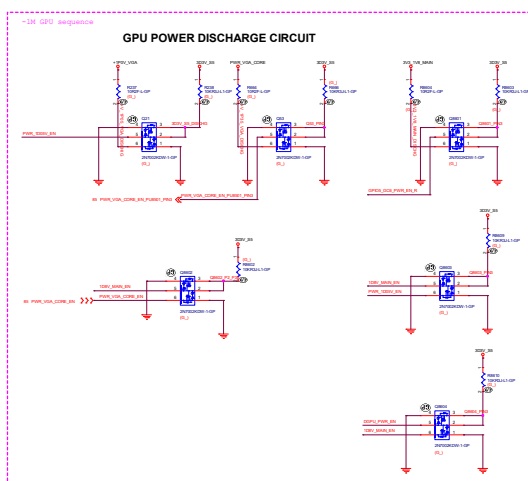
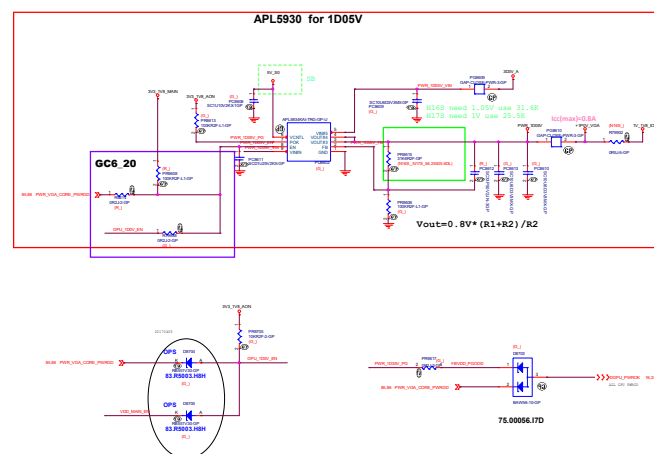
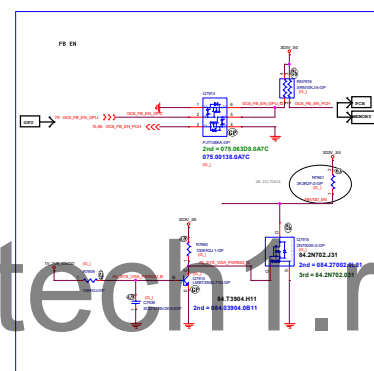
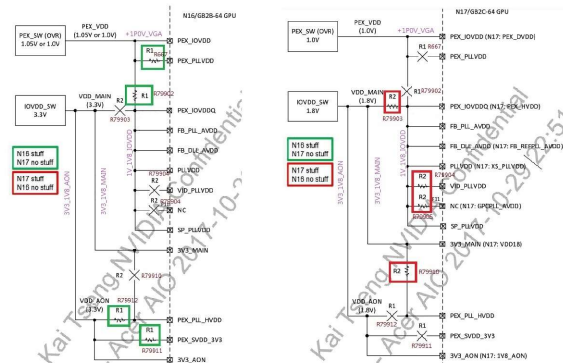
2016/11/17
Dio Yu modify
3V3_IV8_AON
R8514
10KR2J-3-GP
(G_)
R8516
15KR2F-GP
(R_)

2017/04/05
Jimmy JM Wu -1 Modify
依照Power Team建議
PR8525更改为0402 Short pad *

| | PR8524 (F7) | PR8525 (F7) | PC8513 (F7) |
|---------|-------------|-------------|-------------|
| RT8812A | (R_) | (G_) | (G_) |
| RT8812C | (G_) | (R_) | (R_) |

20170210 Jimmy JM Wu Modify
解加壓後會有自動關機的問題。





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| Title GPU Switch | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet 87 of 107 | |

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Title

GPU Switch

Size
A

Document Number

Consumer AIO Petra238i

Rev
1A

Date: Wednesday, July 25, 2018

Sheet 88 of 107

Reserved

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| | | | |
|---|--|---|-----------|
|  | | Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien | |
| Title GPU Others | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet | 89 of 107 |

Reserved

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| | | | |
|---|--|---|-----------|
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| Title NFC | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet | 90 of 107 |

Reserved

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| | | | |
|---|--|---|-----------|
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| Title TPM_(R) | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet 91 of 107 | |

Reserved

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|---|--|---|-----------|
|  | | Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien | |
| Title PS2_(R) | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet | 92 of 107 |

Reserved

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<Core Design>

| | | | |
|---|--|---|-----------|
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| Title Express Card_(R) | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet 93 of 107 | |

Reserved

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Title

Smart Card_(R)

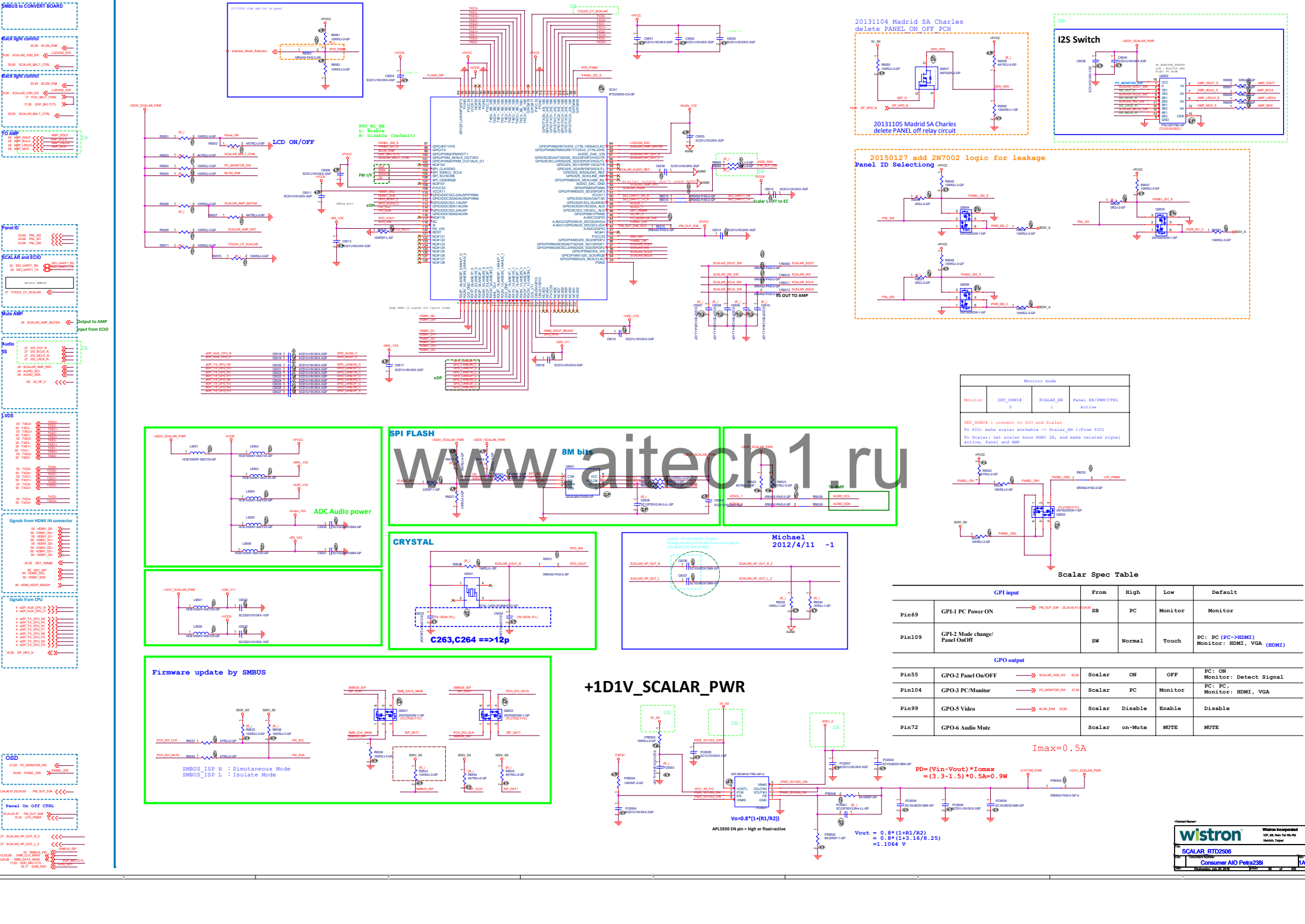
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Document Number
Consumer AIO Petra238i

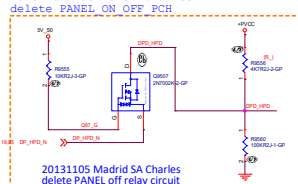
Rev
1A

Date: Wednesday, July 25, 2018

Sheet 94 of 107

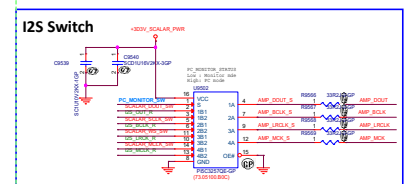


20131104 Madrid SA Charles

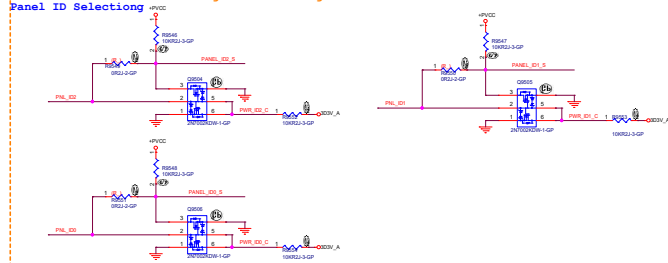


delete PANEL off relay circuit

20131105 Madrid SA Charles

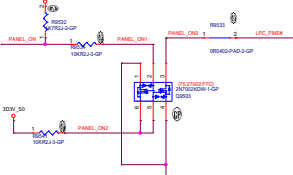


20150127 add 2N7002 logic for leakage



| Monitor mode | | | |
|--------------|-----------|-----------|-------------------|
| Monitor | DET_HDMI# | SCALAR_EN | Panel EN/PWR/CTRL |
| | 0 | 1 | Active |

DET_HDMI# : connect to SIO and Scalar
To SIO: make scalar workable -> Scalar_EN I (from SIO)
To Scalar: let scalar know HDMI IN, and make related signal active, Panel and SIO



Scalar Spec Table

| GPIO input | | From | High | Low | Default |
|-------------|------------------------------|---------------|--------|---------|--|
| Pin69 | GPI-1 PC Power ON | PC_PWR_SW | PC | Monitor | Monitor |
| Pin109 | GPI-2 Mode change/ Panel Off | SW | Normal | Touch | PC: PC (PC->HDMI) Monitor: HDMI, VGA (HDMI) |
| GPIO output | | From | High | Low | Default |
| Pin55 | GPO-2 Panel On/Off | SCALAR_VDD_EN | Scalar | ON | OFF |
| Pin104 | GPO-3 PC/Monitor | PC_MONITOR_SW | Scalar | PC | Monitor |
| Pin99 | GPO-5 Video | BLK_ON_SW | Scalar | Disable | Enable |
| Pin72 | GPO-6 Audio Mute | | Scalar | on-Mute | MUTE |

Imax=0.5A

$P_D = (V_{in} - V_{out}) * I_{max}$
 $= (3.3 - 1.5) * 0.5A = 0.9W$

$V_{out} = 0.8 * (1 + R1/R2)$
 $= 0.8 * (1 + 1.16/8.25)$
 $= 1.1064V$


SSID = SDIO

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| Title Inter LAN_(R) | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet | 97 of 107 |

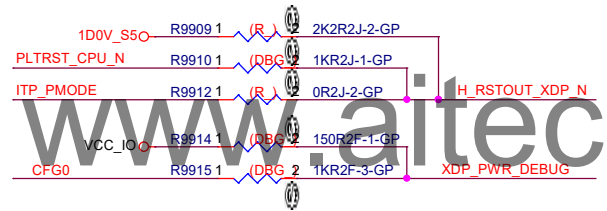
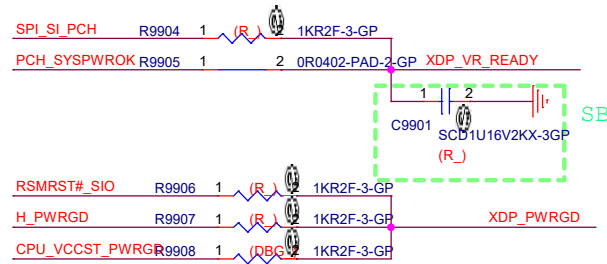
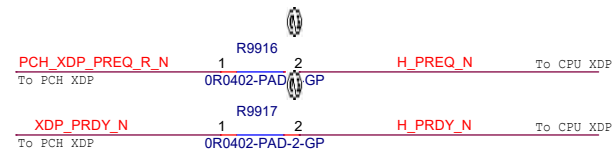
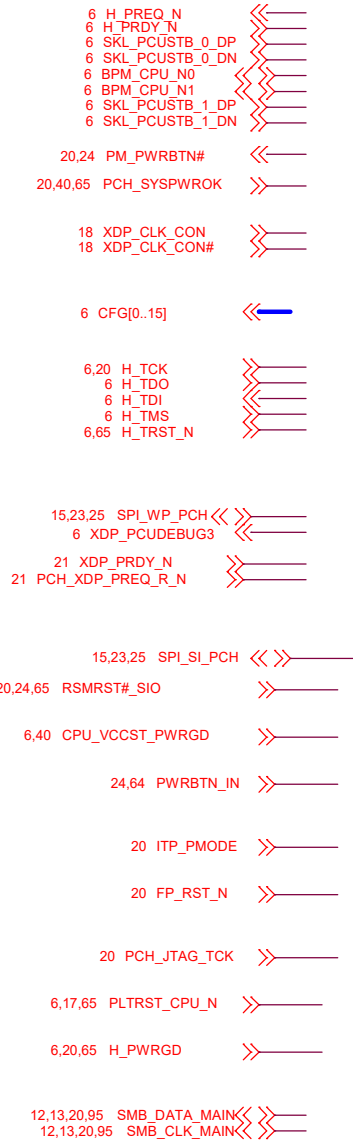
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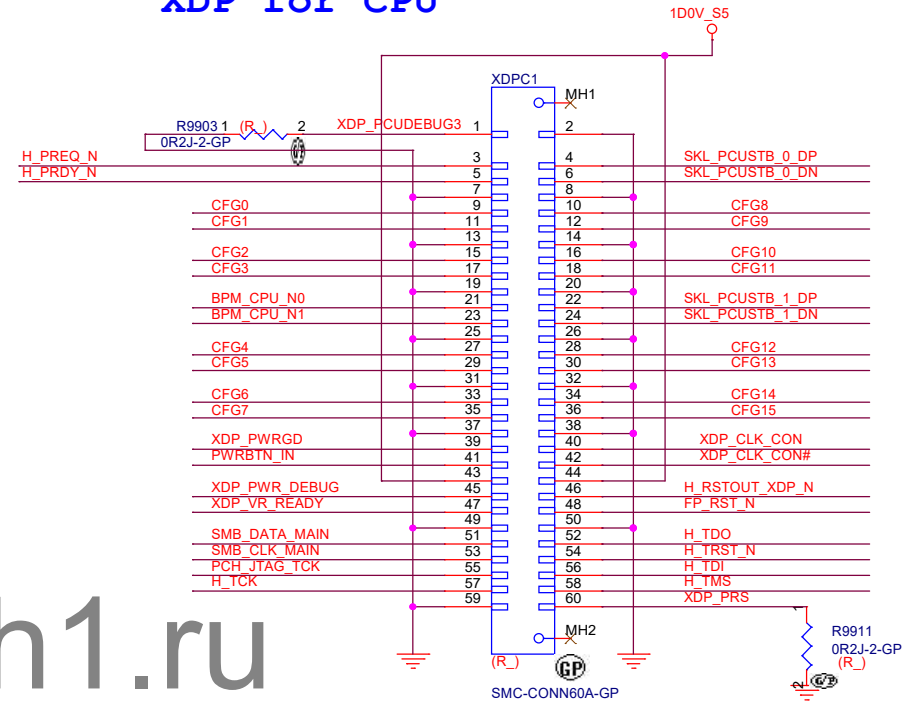
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| Title LAN Switch_(R) | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet 98 of 107 | |

XDP for CPU



XDP for CPU



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| | | | |
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| Title | | XDP&ITP | |
| Size | Document Number | Consumer AIO Petra238i | |
| Custom | Revision | 1A | |
| Date | Wednesday, July 25, 2018 | Sheet | 99 of 107 |

Reserved

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Title

Table of Content

Size
A

Document Number
Consumer AIO Petra238i

Rev
1A

Date: Wednesday, July 25, 2018

Sheet 100 of 107

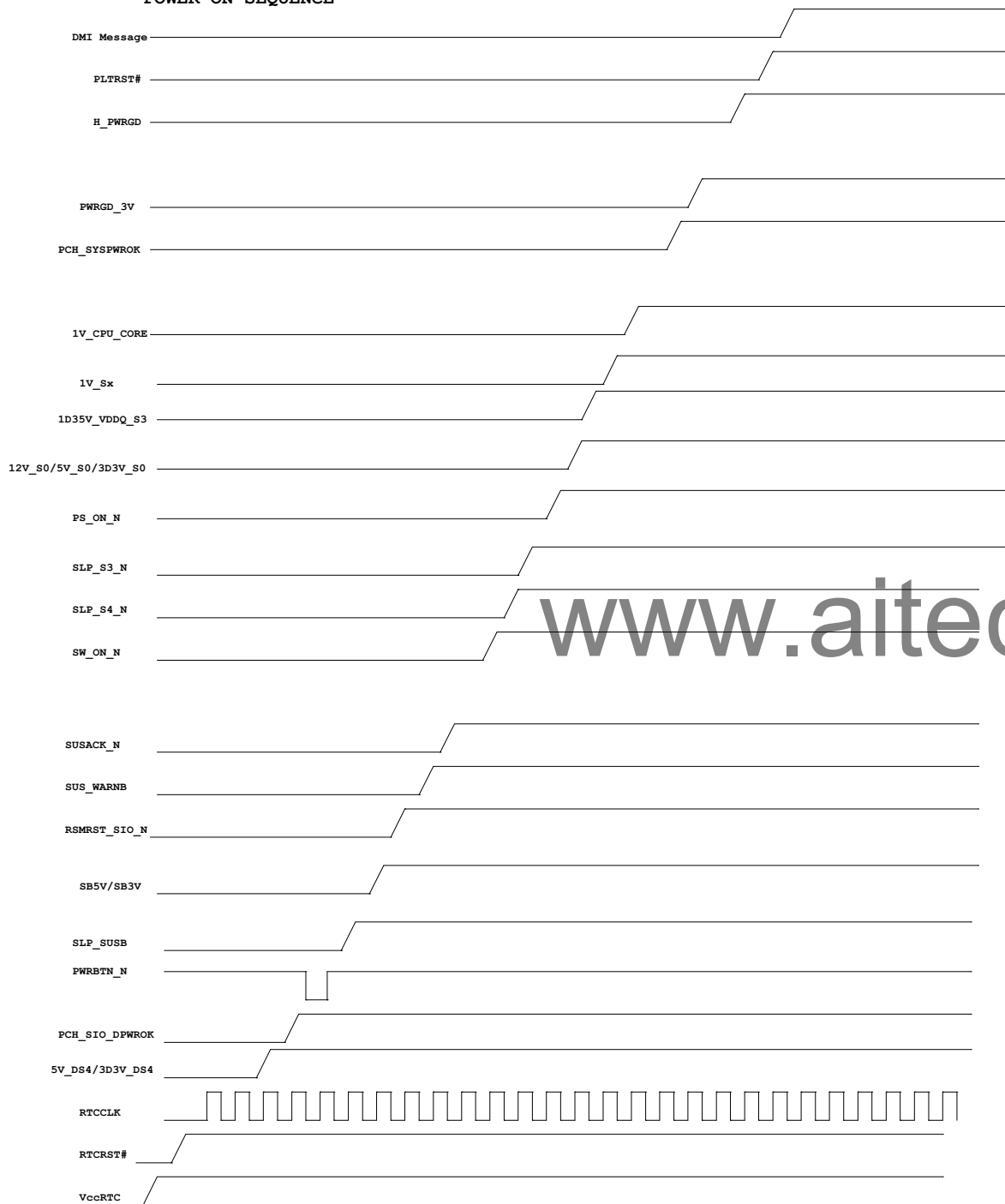
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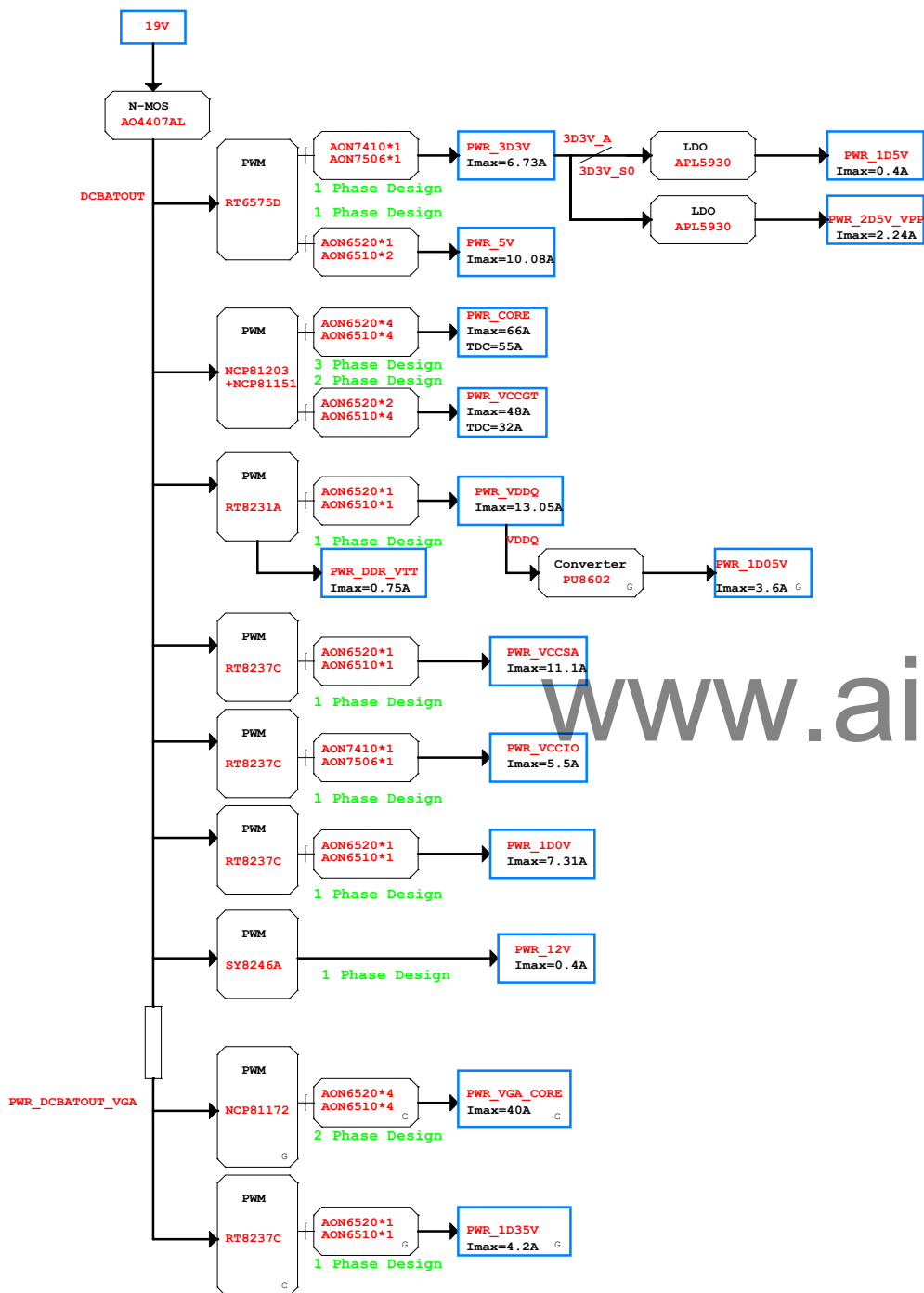
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| Title GPIO table | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet | 101 of 107 |

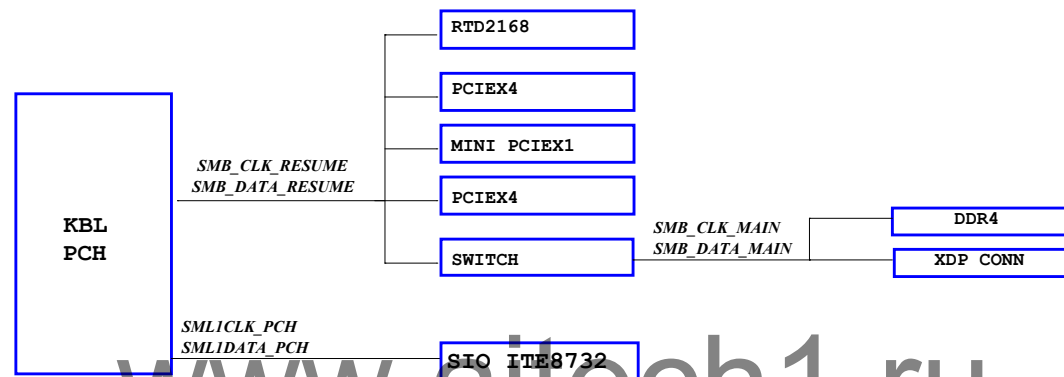
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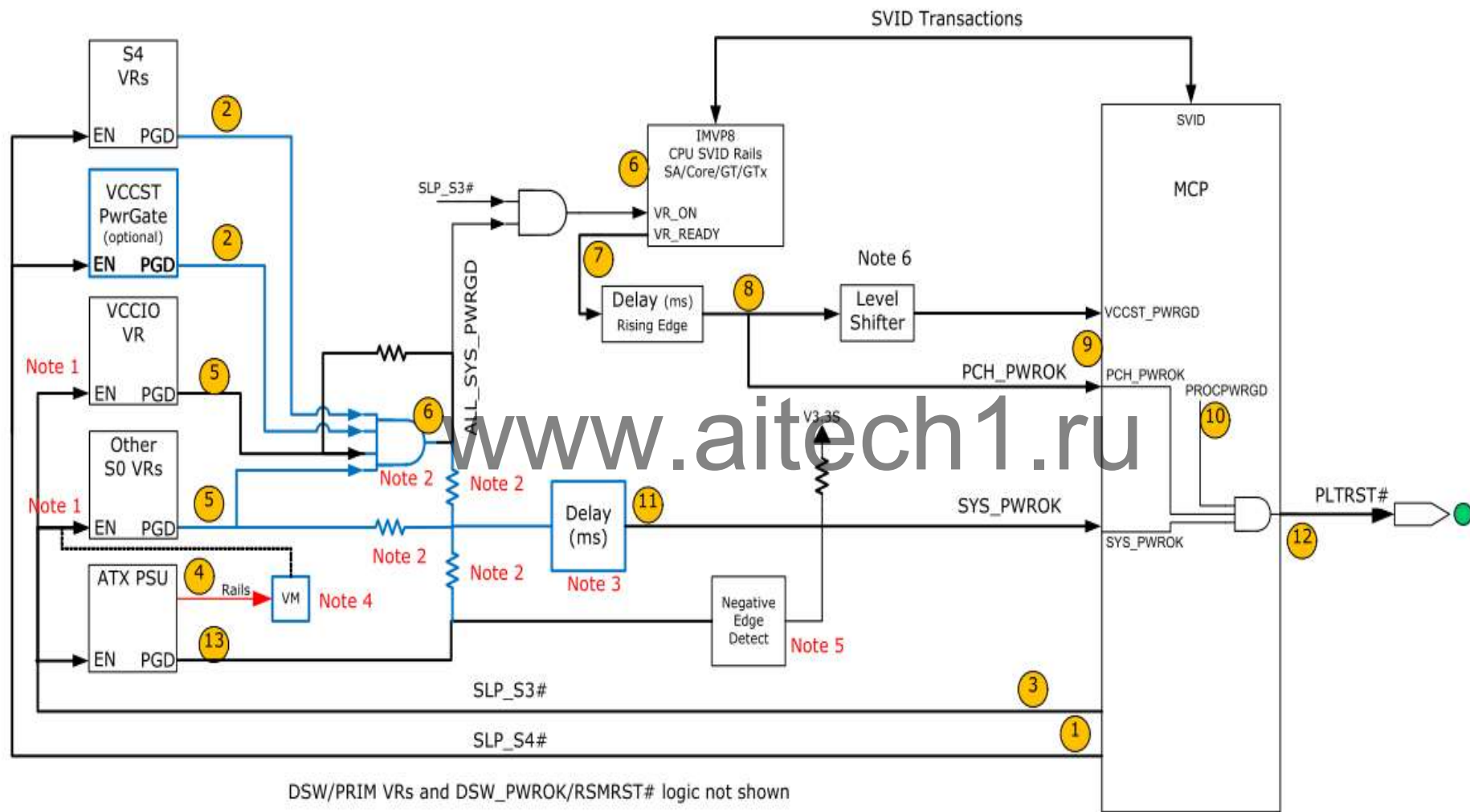


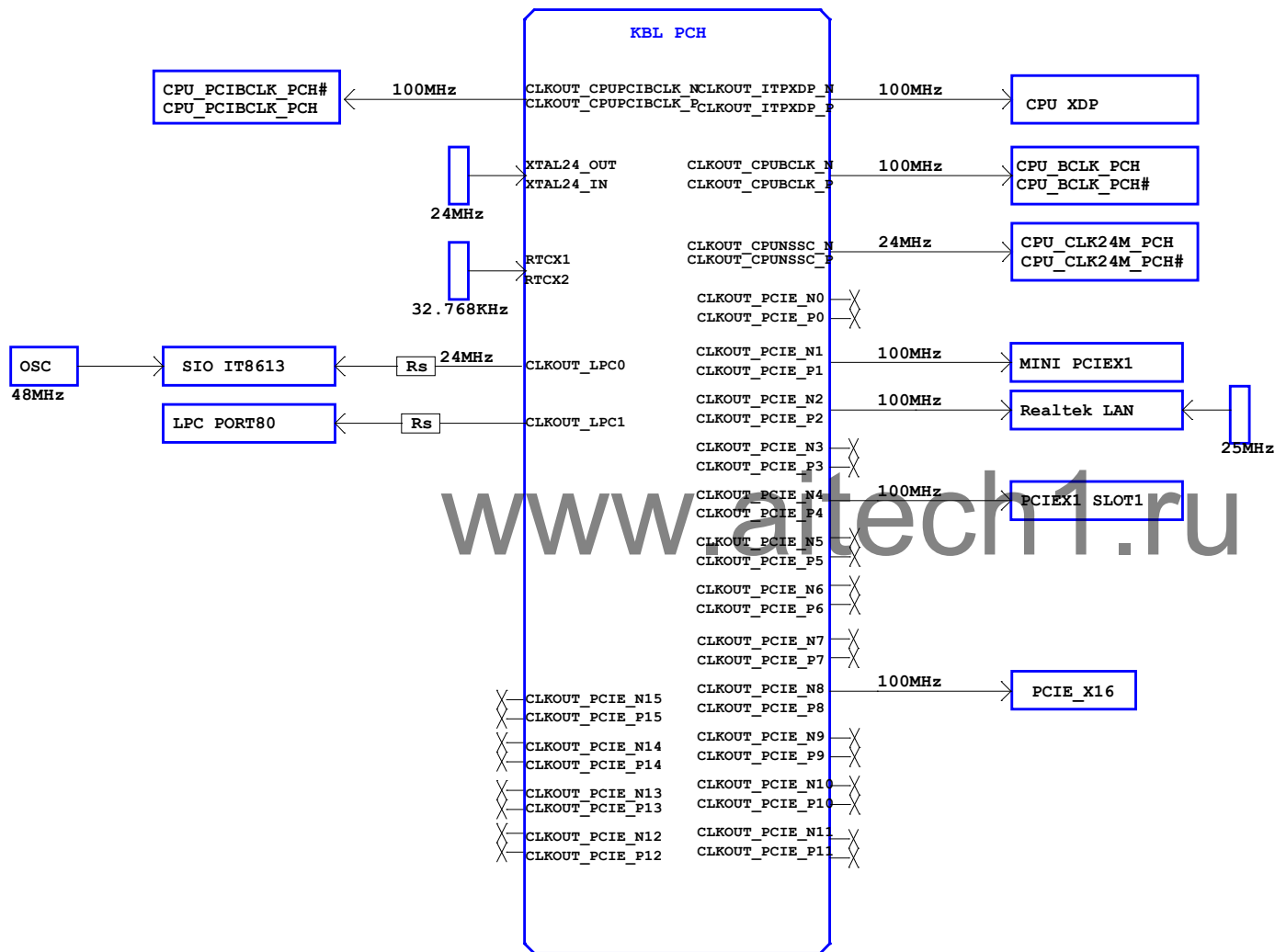
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| Title Other RSVD | | | |
| Size A | Document Number Consumer AIO Petra238i | | Rev 1A |
| Date: | Wednesday, July 25, 2018 | Sheet | 107 of 107 |